PIPD: Power Integrity Path Delay Analysis Tool

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ABSTRACT

IR-drop is a well-known signal integrity issue in very deep submicron technology. The voltage drop does not only induce circuit delay but also reduce the circuit noise margin from lower supply voltage and bring reliability issue from electromigration. PIPD is a gate level path delay analysis tool under insufficient current supplied condition. This tool could help designer fast compute/estimate the longest path delay when occurred voltage drop issues. In this paper, a maximum transition current computation tool is developed. Regard this research past works are pattern independent, which are worst-case predication. Due to the peak current overestimated from above researches, and the accurate peak current is dynamic behavior（pattern dependent）, so we use real functional test bench to activate gate transitions peak current. Our pattern dependent method is more realistic, the measurement results might lower and accurate than past works. Using PIPD could help design reasonable power rail, simulation results prove that our gate-level computation results are very closed to transistor-level simulation results by using HSPICE, the average differ ratios are less than 8%.

Keywords: peak current, voltage drop, path delay

1. INTRODUCTION

Due to the improvement of the technique of integrated circuit in VDSM (Very Deep Sub-Micron) technology; we can use SOC to reduce the cost of hardware and the data processing time. But the VDSM system chip faced some signal integrity issues of IR-Drop, Cross-Talk, and Ground-Bound. Power integrity cause the supply voltage change to produce circuit delay or function fault, also causes the power unpredictable consumption, and reliability problem. Therefore, power integrity becomes the important consideration in deep sub-micron design technology. The IR-Drop (Voltage-drop) rose by the momentary peak current [1-5]. Voltage drop might cause the wrong circuit functionality or performance degradation, and made electromigration phenomenon which affect the reliability. Therefore, during the chip designing procedure, we need not only to guarantee the functionality correct of chip, but also need to more consider power integrity problems such as voltage drop and the disturbance from ground-bounce. The issues mentioned above are occurred by current or voltage changes, thus leads circuit performance impaction problems. The momentary over peak current causes voltage drop question, besides seriously affect delay time to the combinational circuit, it also cause sequential circuit setup/hold time violation. Therefore it is important to pre-discovery the voltage drop might causes the circuit delay question earlier, to reduce the redesign time.

The main reason of voltage drop that came from the insufficient supplied current. each gate not consume the same current due to transistor size, different input pattern and output loading. On the other hand the circuit gate transition times are not same due to the different path delay. So, we general use the same voltage drop for all gate are not realistic, the voltage drop also impact to the circuit delay, make the complex recursive relationship within the indexes of (current, voltage, delay).

Traditional static timing analysis（STA）does not consider the different gate delay when occur varying supply voltage. We find a simple circuit's delay increase up to 14.7% when voltages drop to 0.78Vdd. In this paper, we propose a voltage aware delay calculation framework, which combine the peak current calculation and the path delay induced computation, the methodology will recomputed the path delay, which take the voltage drop factors into consideration. The accurate（current, voltage, delay）library are characterized and calibrated by using HSPICE.

Figure 1 is the pattern dependent linear delay time analysis for a simple circuit.

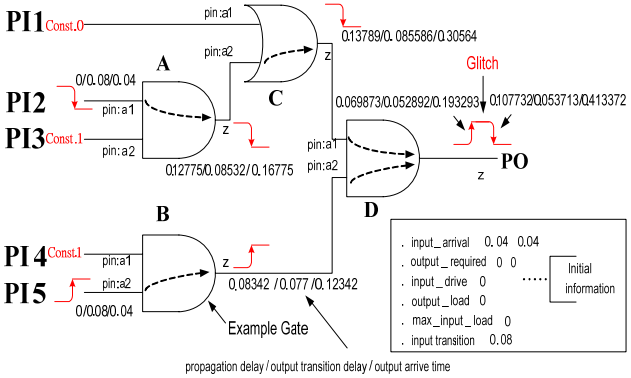

Figure 1: The pattern dependent linear delay analysis.

Figure 2(a) is the current distribution of each logic gate, choose the range of the current produced at the same time. Figure 2(b) is the current summation of each

time slot, sum the current produced at the same time. The real circuit transition current could get by applying the verification input patterns provided by designer.

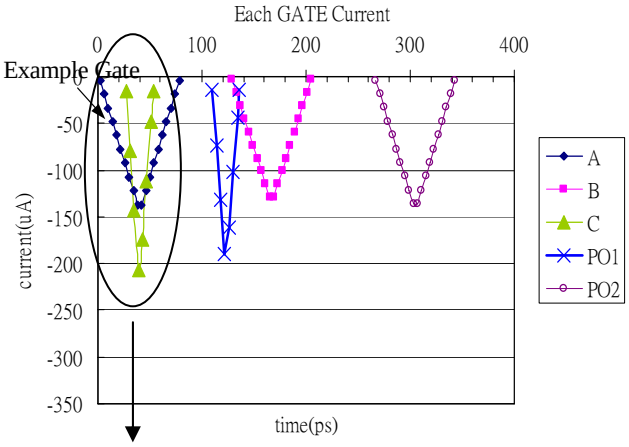

Figure 2(a): current distribution of each logic gate.

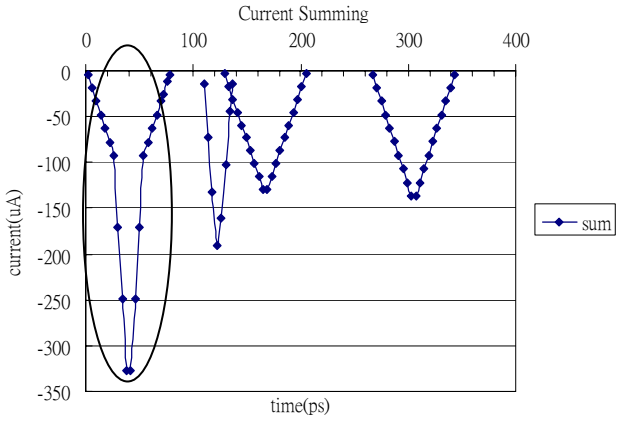

Figure 2(b): the current summation of each time.

2. VOLTAGE-DROP ANALYSIS ALGORITHMS

2.1. DELAY COMPUTATION PROCESS

The voltage drop computation procedure illustration in this section. The program kernel includes non-linear pattern dependent on delay model, the glitch time model. The circuit analysis use the depth first search (DFS) method traverse circuit from the primary input toward to primary output. To compute each node information started from the smallest time in order, the first pattern is used to setup the initial logic value of circuit, the second test pattern to activate the signal transition to simulate the circuit signal delay of circuit. Figure 3 show the circuit delay computation process algorithm. First analysis circuit delay, all logic gates must be analyzed, then calculate the circuit path delay. Sorting the input signal of arrival time in order, simulation circuit logic transition. It needs ignore some logic transition due to glitch signal.

```
Delay Estimation Process（）
{
    Give one pair input pattern
    Search network by DFS
    If first simulate {
      Start point of DFS is 0
    }
    Else {
        start point of DFS decided from voltage
drop estimation process（）
    }
    For each node start from start point {
        Sort the fanin signal arrival time
        For each fanin signal {
        Simulate the node logic in this fanin signal
                    If（the node logic changed） {
   Search gate delay information from cell library
   calculate output delay by non-linear delay model
   Elimination the glitch by the glitch model
                }
        }
    }
}
```

Figure 3: The delay computation process algorithms.

2.2. PEAK CURRENT COMPUTATION PROCESS

This procedure is similar to the circuit delay computation procedure, and could divide into two phases. Phases one is the voltage drop analysis, and the other is the voltage drop analysis. And have to sort different starting point with DFS. Before the voltage drop analysis it wants to count all of the power supply current. After the voltage drop analysis by using the dynamic method to determine and count logic starting point. The starting point is using voltage drop computation procedure to obtain. In the voltage drop computation procedure, we can obtain the logic search starting point. Each time to locate one circuit node, and to analysis current information with the other output of single transition node, to find the generation output transition signal of the input signal. And to catch standard cell library of current information, the current is depend the time point to change current information with any time, and to add each time point of current. Finally, we can obtain the all power supply of current. Figure 4 is peak current computation procedure algorithm. First analysis circuit delay, all logic gates must analysis, then to calculate again that the circuit delay, process gate have logic transition, and pick the information of the current, calculate total current finally.

```
Peak Current Estimation Process( )
{
    Give one pair input pattern
      Search network by DFS
     If first simulate {
          Start point of DFS is 0
    }
     Else {
          start point of DFS decided from voltage
 drop estimation process( )
    }
       For each node start from start point{
       If ( the no de logic changed) {
       Search gate current from cell library
      Summing the current by the input signal arrival
time
      }
    }
}
```

Figure 4: Peak Current Computation Process Algorithm.

2.3. VOLTAGE DROP COMPUTATION PROCESS

After the peak current processing, we can get the peak current of each logic gate. The voltage drop is caused by the insufficient current supplied by current source. So, we use a limited current as the largest peak current to limit and analyze the condition when happen the voltage drops. First, summing the current at each time point. When the peak current value is larger than the limited current (constraint I) at a time point, we use the way of counting real current to find the current value of logic gate. Then, we can find the voltage drop represented by the voltage-current first order linear equation currently. This way of analyzing the effect of the circuit delay by voltage drop, and we can find the circuit delay change, which is only happened after the logic gate affected by the voltage drop. Then, we sort the gates' order by DFS and decided the start point by first index .The sorted DFS to see if this logic gate affected by the voltage drop should be reanalyzed. Repeat the above steps until the peak current value is smaller than the limited current at all time point, then analysis voltage drop effect of current at time (Figure line5). For the voltage drop exceeds maximum limit current of logic gate, to calculate real supply current, and use current -voltage inquiry table to find out voltage drop impaction of gate.

```
Voltage drop Impact delay Computation Process ( )
{
    give the Current Bound ( constrain I )
    set start_time is 0
    for start_time to max_arrival_time{
 if ( peak current at the time interval T larger than Current Bound )  {
            found which gates contribute the peak current at this time interval T
            for each gates {
 re-estimate the supported current
 look up current-to-voltage table to recalculate the real supported voltage
                        }
          sort the gates order by DFS
 decided start point by first index of sorted DFS
 Re-calculate the gate delay by using delay computation process ( )
 Re-calculate the gate current by peak current -computation process ( )
        }
    }
}
```

Figure 5: The voltage drop impact delay computation algorithm.

3.EXPERIMENTAL RESULTS

We develop an accurate gate level voltage drop affect delay analysis tool, the fast gate level result could help designer quickly know the voltage drop impact to performance issue. The delay computation process need compute the peak current of the CUT first, then re-compute the delay timing under the limit current supplied situation.

We obtained the delay analysis under limited supplied for several benchmark-circuits, we use the limit maximum supplied current to emulate the voltage drop condition due to current supplied bound. One pair input patterns are selected from the validation testbench. Table 1, 2 emulates the cases under maximum 100%, 95%, 90%, 85%, 80% current provide to the benchmark circuits. The insufficient current cause voltage drop and the longest path delay time might longer, but especial for some cases are shorter. Designer could apply **PIPD** tools to fast estimate the path delay. It should notice the voltage drop might not certainly degrade the circuit performance. We obtained voltage drop value by HSPICE simulation, analysis longest path delay. We know more limit current would cause the longest path delay increased.

The experimental in Table 1 to 2 to show how serious of delay impacted under supplied current not enough by gate-level computation and transistor-level simulation respectively. The ratio means the supplied largest current (I_{max}) from power unit divided by the peak current (I_{peak}) of the CUT (circuit under test). 100% means $I_{max} = I_{peak}$, the power unit could supply full current as CUT needed, 95 % means $I_{max} = 95\%I_{peak}$, less supplied current might made voltage drop of some gate and increase gate delay problem. The corresponding difference ratio means the largest circuit delay time of under-limit divided by without-limit current condition. We use C432 in Table 1 as example, the longest path delay time increased from 2.63814ns to 2.641302ns due to less 5% current supplied, the corresponding increased ratio is 0.119%. In Table 2, the longest path delay time increased from 2.61568ns to 2.62445ns, the corresponding increased ratio is 0.335%.

We could find the less supplied current might bring voltage drop certain impact to circuit delay increased in most of cases, but not for all circuit. The longest path delay time of C880 circuit, in Table 1 from 2.091796ns decreased to 2.090133ns, in Table 2 from 2.08244ns to 2.08158ns compare the ratio from 90% to 85% respectively.

Table 3 shows our gate-level computation results are very closed to transistor-level computation results, the average differ ratios are less than 8%.

4.CONCLUSION

We develop an efficient gate level voltage drop affect delay calculation tool, which could fast to estimate the gate level estimation result to help designer quick know the voltage drop impact path delay condition. We also could know the voltage drop not certain impact to circuit delay.

5. REFERENCE

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Table 1: The gate-level longest path delay time under voltage drop（Ours）

		Maximum current supplied ratio（%）					Corresponding difference ratio（%）			
Circuit Name	Approx. Gate Count	100%	95%	90%	85%	80%	95%	90%	85%	80%
C432	169	2.638154	2.641302	2.64911	2.657874	2.662982	0.119	0.415	0.747	0.941
C499	422	2.014038	2.01585	2.016533	2.017679	2.02086	0.09	0.124	0.181	0.339
C880	367	2.087673	2.086693	2.091796	2.090133	2.096792	-0.047	0.197	0.118	0.437
C1908	654	2.774848	2.776598	2.779952	2.781251	2.785273	0.063	0.184	0.231	0.376
C2670	789	2.248779	2.248779	2.248779	2.248779	2.248779	0	0	0	0
C3540	1268	3.52456	3.52456	3.535223	3.537107	3.541319	0	0.303	0.356	0.475
ALU4	610	3.427479	3.441253	3.449304	3.457876	3.460882	0.402	0.637	0.887	0.975
COUNT	95	2.054855	2.073416	2.058397	2.062151	2.066446	0.903	0.172	0.355	0.564
DALU	1662	3.183363	3.185428	3.204508	3.277547	3.310994	0.065	0.664	2.959	4.009
DECOD	37	0.33642	0.341569	0.34378	0.347521	0.351532	1.531	2.188	3.3	4.492
F51M	131	0.648551	0.65431	0.657122	0.660915	0.661779	0.888	1.322	1.906	2.040
MAJORITY	7	0.438354	0.440379	0.441422	0.444919	0.445509	0.462	0.700	1.498	1.632
MY_ADDER	191	1.75167	1.752219	1.754162	1.759866	1.759068	0.031	0.142	0.468	0.422
PARITY	45	0.634721	0.638179	0.639723	0.64047	0.643745	0.545	0.788	0.906	1.422
Z4ML	62	0.63161	0.63161	0.63161	0.63161	0.63161	0	0	0	0

Unit：ns

Table 2: The Transistor-level longest path delay time under voltage drop effect（HSPICE）

		Maximum current supplied ratio（%）					Corresponding difference ratio(%)			
Circuit Name	Transistor Count	100%	95%	90%	85%	80%	95%	90%	85%	80%
C432	920	2.61568	2.62445	2.657	2.68317	2.71288	0.335	1.58	2.58	3.716
C499	1984	1.85939	1.87758	1.88464	1.89844	1.91642	0.978	1.358	2.1	3.067
C880	1652	2.0646	2.07982	2.08244	2.08158	2.08766	0.737	0.864	0.822	1.117
C1908	2800	2.30886	2.33056	2.34233	2.35434	2.38889	0.94	1.45	1.97	3.466
C2670	3968	2.1174	2.11987	2.12321	2.12871	2.13337	0.117	0.274	0.534	0.754
C3540	5866	3.33517	3.36632	3.36875	3.38818	3.40254	0.934	1.007	1.589	2.02
ALU4	3066	3.15199	3.21977	3.2669	3.30785	3.393	2.15	3.646	4.945	7.646
COUNT	570	1.89823	1.92332	1.90723	1.9143	1.91847	1.322	0.474	0.847	1.066
DALU	7900	3.25872	3.43414	3.55496	3.7345	3.873	5.383	9.091	14.6	18.850
DECOD	176	0.35593	0.37937	0.3954	0.40672	0.41949	6.586	11.089	14.27	17.857
F51M	544	0.69278	0.72276	0.73775	0.75644	0.79733	4.327	6.491	9.189	15.091
MAJORITY	38	0.42493	0.43603	0.4426	0.44569	0.4672	2.612	4.158	4.886	9.948
MY_ADDER	800	1.59671	1.60872	1.6057	1.61021	1.60691	0.752	0.563	0.845	0.639
PARITY	240	0.6559	0.67226	0.68224	0.68366	0.69776	2.494	4.016	4.232	6.382
Z4ML	252	0.65315	0.65417	0.6519	0.65395	0.65372	0.156	-0.191	0.122	0.087

Unit：ns

Table 3: The longest path delay time comparison after voltage drop

	Our V.S. HSPCIE differ ratio（%）			
Circuit Name	95%	90%	85%	80%
C432	0.642	0.297	0.943	1.839
C499	7.364	6.998	6.281	5.450
C880	0.330	0.449	0.411	0.437
C1908	19.139	18.683	18.133	16.593
C2670	6.081	5.914	5.640	5.410
C3540	4.701	4.942	4.395	4.079
ALU4	6.879	5.583	4.535	2.001
COUNT	7.804	7.926	7.724	7.713
DALU	7.242	9.858	12.236	14.511
DECOD	9.964	13.055	14.555	16.200
F51M	9.471	10.929	12.628	17.001
MAJORITY	0.997	0.266	0.173	4.643
MY_ADDER	8.920	9.246	9.294	9.469
PARITY	5.070	6.232	6.317	7.741
Z4ML	3.449	3.112	3.416	3.382
Average	6.537	6.899	7.112	7.765