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Advanced MOSFET Technologies

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中文摘要

多方功能性與複雜性的積體電路組合近來增加的很快速。在 1990 年後，藉著縮小的元件和線寬的尺寸這些複雜的特性被完成，且還需要去藉著使用較低電阻值的銅去取代鋁合金來降低電路延遲。

電致遷移(EM)，金屬的質量傳輸是由於導電的電子和擴散金屬原子之間的動能轉換，和存在的電流流通在金屬導線上。電致遷移已經在 100 年多前就已經被大量的發現，1996 年的早期的 IC 製造出來的時期是它第一次被揭發和持續有問題出現。電致遷移是未來在後段製程研究的主要影響因素。

另外，在這 20 年來，應力通道技術被完全檢驗，因為它增強了載子在元件驅動電流移動的主要因素的貢獻。為了 CMOS 高的效能，近來他有被提出整合入積體電路工業裡。雖然有很多的方法去尋找高增強型的元件，但應力技術是很有希望的候選者之一。接下來的章節我們將探討在一般(100)矽基板的矽通道的應力。我們將討論基本的矽應力的物理機制、近來提出的技術和未來的目標。

互補式金氧半製程是最重要的半導體積體電路技術，舉凡記憶體及邏輯等多樣化的產品皆以此作為發展的原動力，相關產業也因而興盛不已。一個 MOS 電晶體元件是以閘極作為控制電極，即以閘極的電壓訊號控制電晶體的輸出特性。傳統上，是以含高濃度 n 型雜質的多晶矽做為此閘極材質。進入深次微米紀元後，相關的閘極技術有很大的變革，也面臨許多的挑戰及問題待突破與解決，包括材料種類、形成方式、及可靠性等。

除了以上簡短說明之外，此報告將還會針對 MOSFET 應用方面，如無電鍍化學、Flash、奈米科技的應用・・・等等作更深一步的探討。

關鍵字：Electromigration、Strain、FUSI、Electroless plating、Flash、Nanowires.

English Abstract

Functionality and complexity of circuit components in integrated circuits have recently increased rapidly. These complex features have been achieved by reduction in the dimensions of both the devices and wiring. In the 1990s, the need to reduce circuit delays prompted the replacement of Al alloy with lower resistivity Cu.

Electromigration (EM), the mass transport of a metal due to the momentum transfer between conducting electrons and diffusing metal atoms, and the current flows exist and through metal wires. The electromigration was discovered more than 100 years ago, it first showed up in ICs as early as 1966 and has been a persistent problem since the early days of IC manufacturing. The electromigration is mainly factor to study for backend process in future.

Further, the strained channel technology has been examined over twice decades because it enhances the carrier mobility contributing to the device drive current. Recently It has be proposed to be integrated into integrated circuit industry for the CMOS higher performance. Although there are many methods to seek for higher device performance enhancement, but the strain technology is the promising candidate. In this chapter we will focus on the strained silicon channel on general (100) silicon wafer. We will discuss the fundamentals of strained silicon physic mechanism, the recent proposed technology and the future work.

A study of the implementation of FUSI gates to scaled devices is presented, addressing the issue of phase control at short gate lengths. A linewidth effect for Ni FUSI gates is found for non-optimized processes targeting NiSi, with formation of NiSi at long gate lengths and Ni-rich silicides at short gate lengths. This is attributed to Ni diffusion from areas surrounding the gates, resulting in a larger reacted Ni-Si ratio at short gate lengths. The linewidth dependence of the Ni FUSI phase results in an undesirable kink in the Vt roll-off characteristics, due to the difference in effective work function between the Ni silicide phases, which is particularly large for HfSiON dielectrics. An optimized 2-step RTP silicidation process is shown to eliminate this problem allowing the formation of NiSi gates uniformly at all gate lengths. The application and scalability of Ni-rich silicides to PMOS devices is also demonstrated, as well as a scheme for CMOS integration of dual WF phase

controlled FUSI, using an etch back step to reduce the poly-Si height on PMOS electrodes before full silicidation.

Except as above brief description, the paper will continued focus the application for MOSFET device, as electroless plating, flash, nanowires technology…etc, and it will discuss them detailed.

Key Word: Electromigration、Strain、FUSI、Electroless plating、Flash、nanowires.

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Chapter 1 Electromigration

1.1 Introduction

When electrons flow through wires on a chip, they collide with metal atoms, producing a force on the atoms, exists wherever wires break over the chip's lifetime. When early ICs were returned from the field and examined under a microscope, very fine "cracks" in the wires were found. To avoid the damages that which make the metal wires thicker. Making wires thicker was easy when they were 10 microns wide, but it can't satisfy today's 90 nanometer and 65 nanometer technologies.

The conditions necessary for electromigration to be a significant problem continue to bear down on us with increasing speed → high current densities, long narrow wires, logic hazards, and high operating frequencies. The transition was solved the electromigration problem from aluminum wires to copper wires. The copper has made electromigration analysis of chips more complex in fact. Reduced wire size in both width and thickness and higher frequencies continue to push the current densities wires can handle. Wire slotting and via haracteristics in copper also lead to more complex design rules for electromigration.

Let us briefly examine the advantages for using Cu and arrive at some feel for the driving force for its use. Cu has a room-temperature resistively about 60% that of Al. Naively, this might lead one to think that a substantial increase in speed may be achieved by its use, but careful analyses indicate that the benefit realized from the lower resistance is minimal. Therefore the primary benefit for the replacement of Al-base alloys with Cu is for reliability purposes and the reduction of electromigration-induced damage in the higher melting point slower-diffusing metal. In addition, if the reliability did not alloy an increase in the current density, the benefit is hardly realized, since the processing of Cu alloy is so much more difficult at this time, therefore it is more appropriate when comparing competing metallurgical schemes, to speak of increase allowable current density and not of increased lifetime.

The IC designers need tools that can find and help fix eletromigration problems during the design stage before they become problems in silicon.

At the high current densities typical in thin-film conductors on integrated circuits, there is significant momentum transfer from the electrons to the atoms. The microstructure of the metallization leads to the consequent atomic flow being non-uniform, and damage results in the form of voids or hillocks.

The temperature and electron wind force are main factor for electromigration.

1.1.1 History

The phenomenon of electromigration has been known for over 100 years, having been discovered by the French scientist Gerardin.

The topic first became of practical interest in 1966 when the first integrated circuits became commercially available.

In this field, the research was pioneered by James R. Black, who set the basis for all research in this area and after whom Black's law (Black's equation) is named. As below Fig. 1.

Black's Equation：

$$MTTF = Aj^{-n}e^{\left(\frac{Q}{kT}\right)}$$

MTF is a mean time to failure,

A is a constant

j is the current density

n is a model parameter

Q is the activation energy in eV (electron volts)

k is Boltzmann constant

T is the absolute temperature in ˚K

Fig. 1: Black`s Equation

1.1.2 Practical implications of EM

The phenomenon of electromigration will let metal line to open or short.

At the time the metal interconnects in ICs were still about 10 micrometres wide. Currently interconnects are only micrometres or nanometers in width making research in electromigration increasingly important.

Electromigration was identified first as a serious reliability concern on the Al-based integrated circuit (IC) in 1967. More than thirty years later, electromigration remains a dominant reliability concern for the modern IC due to the aggressive decrease of interconnect dimensions and the comparably aggressive increase of current densities required during operation (Fig. 2).

Simultaneously, the need to lower capacitance in the interconnect system in order to further decrease RC-delay has motivated the implementation of low-k inter-level dielectric (ILD) materials in place of the traditional SiO2-based material (Fig. 3).

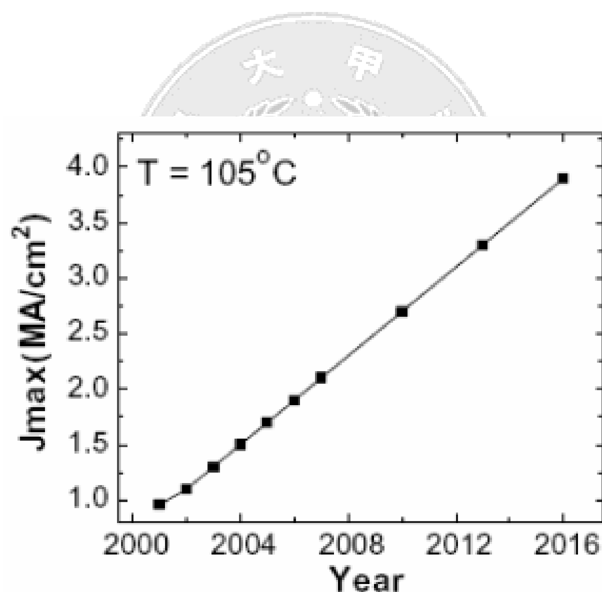


Fig. 2 The requ1red current density at operating conditions continues to rise with time as depicted by the International Technology Roadmap for Semiconductors, 2002 edition.

【Christine S. Hau-Riege, An introduction to Cu electromigration, 20 October 2003, p2】

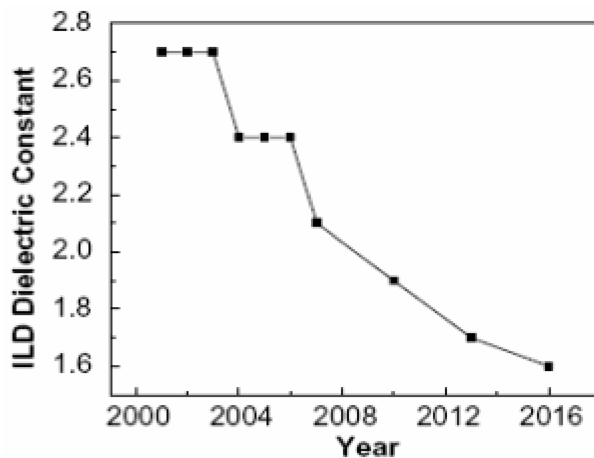


Fig. 3 The minimum effective dielectr1c constant needed for the continuous decrease in RC-delay, as depicted by International Technology Roadmap for Semiconductors, 2002 edition.

【Christine S. Hau-Riege, An introduction to Cu electromigration, 20 October 2003】

1.1.3 Fundamentals

The characteristics are predominantly:

- The composition of the metal alloy.
- The dimensions of the conductor.

The shape of the conductor:

- The crystallographic orientation of the grains in the metal.
- The layer deposition.
- Heat treatment or annealing.
- The passivation characteristics.
- The interface to other materials.

→ As above, there are affected the durability of the interconnect lines.

The time dependent current:

- Direct current.
- Alternating current.

Forces on ions in an electrical field:

- Two forces affect ionized atoms in a conductor. The direct electrostatic force “Fe” as a result from the electric field. The force from the exchange of momentum with other charge carriers “Fp” showing toward the flow of charge carriers. In metallic conductors “Fp” is called “electron wind” or “Ion wind”.
- The resulting force “Fres” on as activated ion in the electrical field is

$$F_{res} = F_e - F_p = q \cdot Z^* \cdot E = q \cdot Z^* \cdot j \cdot \rho$$

- The electromigration occurs when some of the momentum of a moving electron is transferred to a nearby-activated ion. This causes the ion to move from its original position. Over time this force knocks a significant number of atoms from their original positions. A break or gap can develop in the conducting material, preventing the flow of electricity. In the narrow interconnect conductors, such as those linking transistors and other components in integrated circuits, this is known as a void or internal failure open circuit (as Fig. 4 and Fig. 5)). The electromigration can also induce the atoms of a conductor to pile up and drift toward other nearby conductors, creating an unintended electrical connection known as a hillock failure or whisker failure (short circuit, as Fig. 6 and Fig. 7). Both of these situations can lead to a malfunction of the circuit.

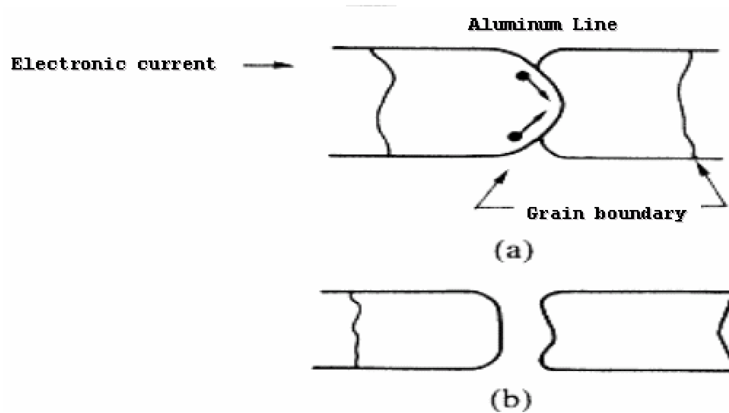


Fig. 4 the atomics of aluminum were movement along grain boundary in electronic field.

【羅仁聰,半導體銅導線之電子及應力遷移可靠度探討,交通大學機械系, 2005】

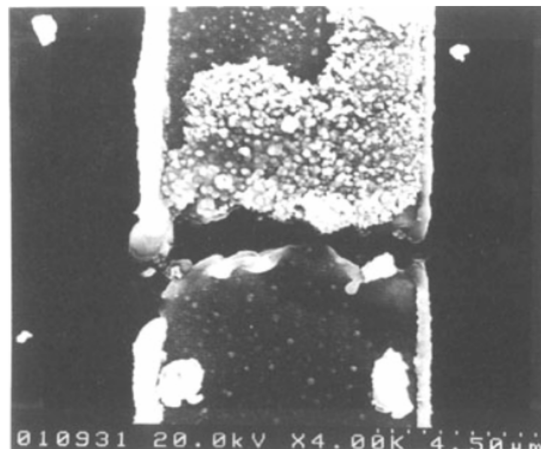


Fig. 5 Electromigration induces the void and hillock.

【吳文發、秦玉龍, NDL 奈米通訊,第六卷第一期, 電遷移效應對銅導線可靠度之影響】

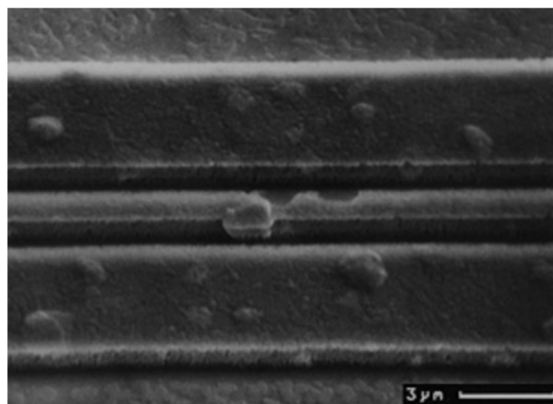


Fig. 6 SEM micrograph showing voids and hillocks.

【http://www.msm.cam.ac.uk/mkg/e_mig.htm】

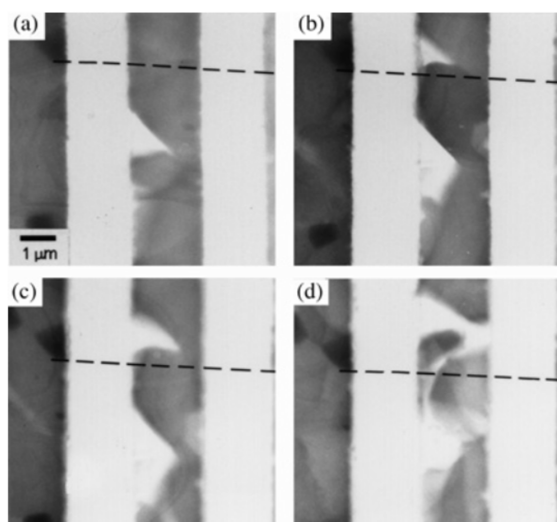


Fig. 7 TEM micrographs of in-situ test showing voiding.

【http://www.msm.cam.ac.uk/mkg/e_mig.htm】

1.1.4 Failure mechanisms

- Diffusion mechanisms:
  - In a homogeneous crystalline structure, because the uniform lattice structure of the metal ions, there is hardly any momentum transfer between the conduction electrons and the metal ions. However, this symmetry does not exist at the grain boundaries and material interfaces, and here momentum is transferred much more vigorously. Since the metal ions in these regions are bonded more weakly than in a regular crystal lattice, once the electron wind has reached certain strength, atoms become separated from the grain boundaries and are transported in the direction of the current. This direction is also influenced by the grain boundary itself, because atoms tend to move along grain boundaries.
  - Diffusion processes caused by electromigration can be divided into grain boundary diffusion, bulk diffusion and surface diffusion. In general, grain boundary diffusion is the major electromigration process in aluminum wires, whereas surface diffusion is dominant in copper interconnects.

- Grain boundary diffusion: (as Fig.8 and Fig.9)
  - We have been studying a new class of defects called the grain boundary diffusion wedges in polycrystalline thin films. These diffusion wedges are formed by stress driven mass transport between the free surface of the film and the grain boundaries during the process of substrate-constrained grain boundary diffusion. The mathematical modeling involves solution to integro-differential equations representing a strong coupling between elasticity and diffusion. We show that the solution can be decomposed into diffusional eigenmodes reminiscent of crack-like opening displacement along the grain boundary that which leads to a singular stress field at the root of the grain boundary. We find that the theoretical analysis successfully explains the difference between the mechanical behaviors of passivated and unpassivated copper films during thermal cycling on a Si substrate.
  - An important implication of our theoretical analysis is that

dislocations with Burgers vector parallel to the interface can be nucleated at the root of the grain boundary. This is a new dislocation mechanism in thin films that which contrasts to the well-known Mathews-Freund-Nix mechanism of threading dislocation propagation. Recent TEM experiments at the Max Planck Institute have shown that, while threading dislocations dominate in passivated metal films, parallel glide dislocations dominate in unpassivated copper films with thickness below 400nm. This is fully consistent with our theoretical predictions.

- Bulk difference: (as Fig. 10)
  - Bulk diffusion, the concentration of metal particle is zero momentum when the surface material have been coating. Base on difference concentration, the metal particle of the PR film diffuses to surface material.

- Surface diffusion: (as Fig. 11)
  - Diffusion of adsorbates is an important elementary step of many surface processes such as epitaxial growth or catalytic reactions. Usually, surface diffusion is a thermally activated process that is initiated by heating the substrate. In some cases it would be desirable to enable diffusion at a lower temperature where competing surface reactions have not yet set in. For this and other purposes one would like to induce diffusion by electronic instead of thermal excitation similar to the well studied phenomena of desorption induced by (multiple) electronic transitions.

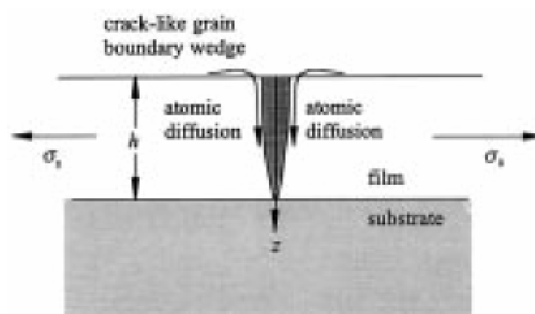


Fig. 8 we have a class of defects called the grain boundary diffusion wedges in polycrystalline thin films.

【H.GAO, L.ZHANG, W.D.NIX, C.V.THOMPSON and E.ARZT, Crack-Like Grain-Boundary Diffusion Wedges in Thin Metal Films, 22 May 1999】

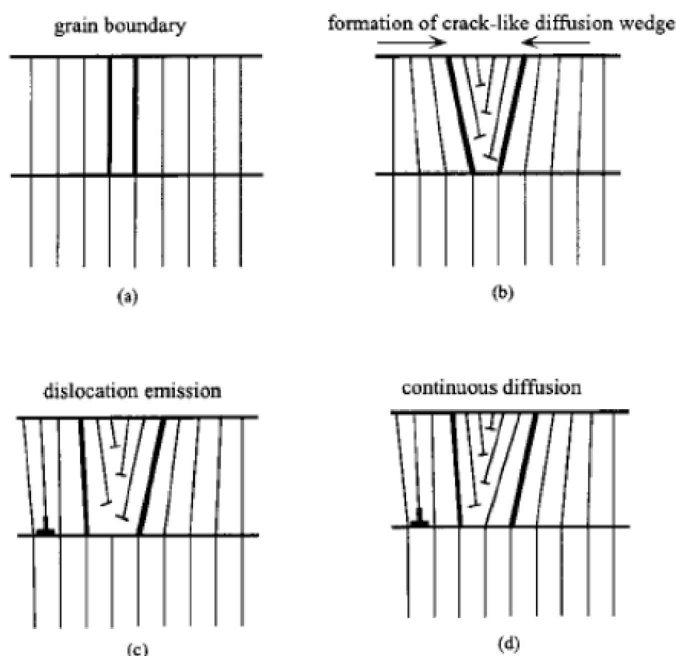


Fig. 9 The phenomenon usual occurs at which dislocation.

【H.GAO, L.ZHANG, W.D.NIX, C.V.THOMPSON and E.ARZT, Crack-Like Grain-Boundary Diffusion Wedges in Thin Metal Films, 22 May 1999】

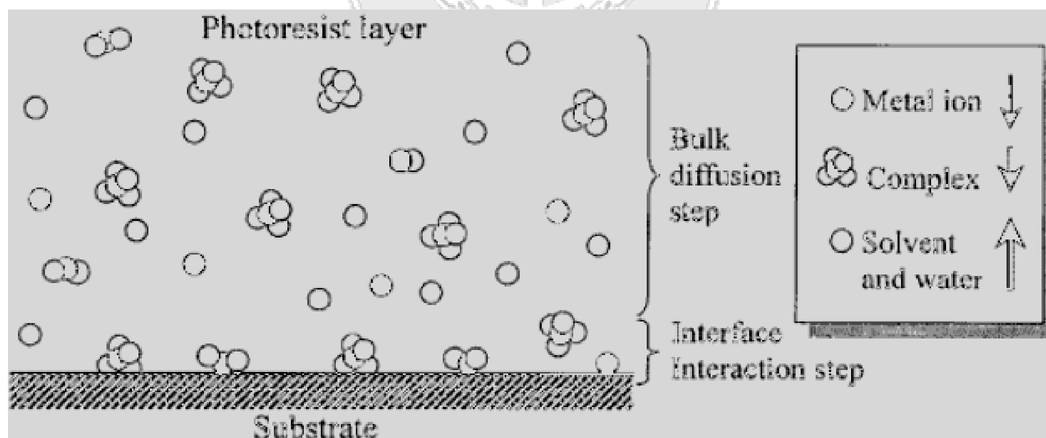


Fig. 10 Bulk diffusion is the global macro-motion of the material within the deposited layer.

【楊金成、柯富祥、王美雅、王天戈, NDL 奈米通訊-第六卷第四期, 金屬雜質於 DUV 光阻中擴散及吸附行為之研究(I)】

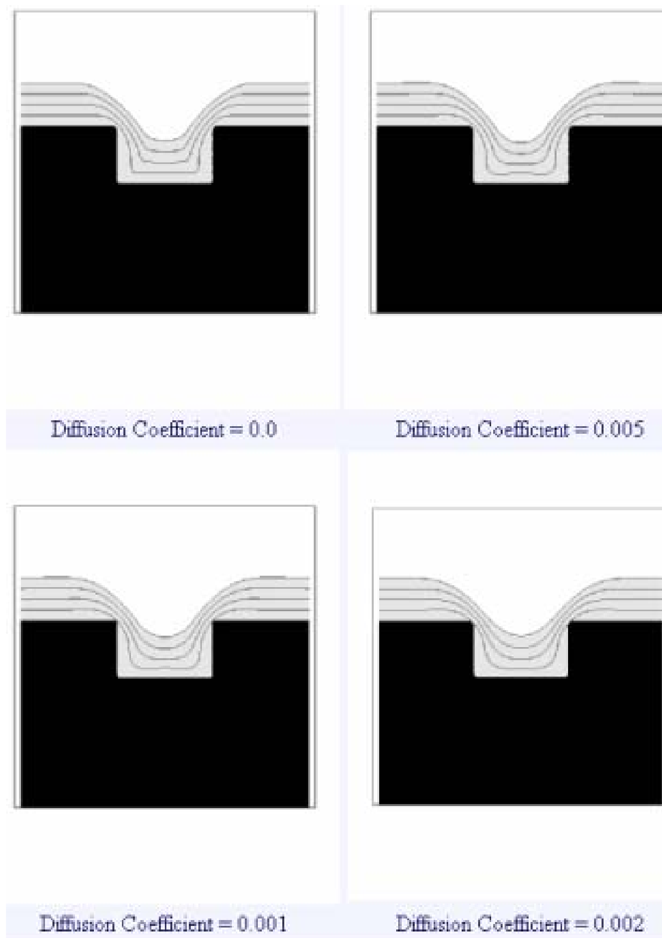


Fig. 11 Surface diffusion relates to the motion of metal boundaries. Diffusion of adsorbates is an important elementary step such as epitaxial growth or catalytic reactions. Usually, surface diffusion is a thermally activated process that is initiated by heating the substrate.
【http://math.berkeley.edu/~sethian/2006/Semiconductors/ieee_surface_diffusion.html】

- Thermal effects: (as Fig. 12 and Fig. 13)
  - In an ideal conductor, the atoms are arranged in a perfect lattice structure, the electrons moving through it would experience no collisions and electromigration would not occur. In real conductors, the defects in the lattice structure and the random thermal vibration of the atoms about their positions causes electrons to collide with the atoms and scatter, that is the source of electrical resistance. Normally, the amount of momentum imparted by the relatively low-mass electrons is not enough to permanently displace the atoms. Anyway, in high-power situations (such as with the increasing current draw and decreasing wire sizes in the VLSI microprocessors); enough

electrons bombard the atoms with enough force to become significant. Or, the process of electromigration accelerates by causing the atoms of the conductor to vibrate further from their ideal lattice positions, increasing the amount of electron scattering. High current density increases the number of electrons scattering against the atoms of the conductor, and hence the speed at which those atoms are displaced.

- In integrated circuits, electromigration does not occur in semiconductors directly, but in the metal interconnects deposited on them.
- Electromigration is exacerbated by high current densities and the Joule heating of the conductor, and it can lead to eventual failure of electrical components. Localized increase of current density is known as current crowding.

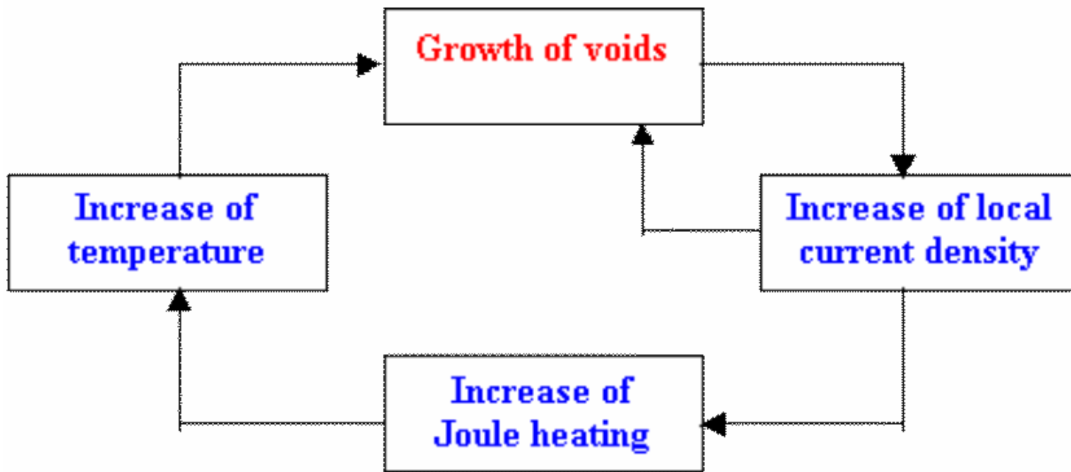


Fig. 12 Thermal induced electromigration effect.

【CSL, 2005, http://www.csl.mete.metu.edu.tr/Electromigration/emig.htm】

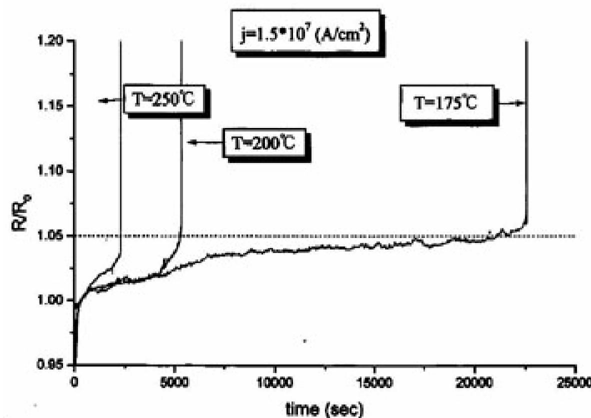


Fig. 13 Base on difference temperature, variation ratio of time vs. resistance for electromigration effect.

【吳文發、秦玉龍, NDL 奈米通訊-第六卷第一期, 電遷移效應對銅導線可靠度之影響】

- Balance of atom concentration:
  - A governing equation which describes the atom concentration evolution throughout some interconnect segment, that is the mass balance (continuity) equation

$$\frac{\partial N}{\partial t} + \nabla \cdot \vec{J} = 0$$

Where $N(\vec{x}, t)$ is the atom concentration at the point with a coordinates $\vec{x} = (x, y, z)$ at the moment of time t, and J is the total atomic flux at this location. The total atomic flux J is a combination of the fluxes caused by the difference atom migration forces. The major forces are induced by the electric current, and by the gradients of temperature, mechanical stress and concentration. $\vec{J} = \vec{J}_c + \vec{J}_T + \vec{J}_\sigma + \vec{J}_N$. Define the fluxes mentioned above. $\vec{J}_c = \frac{NeZD\rho}{kT}\vec{j}$. Here e is the electron charge, eZ is the effective charge of the migrating atom, ρ the resistively of the conductor where atom migration 'takes place', $\vec{j}$ is the local current density, k is Boltzmann's constant, T is the absolute temperature. $D(\vec{x}, t)$ Is the time and position dependent atom diffusivity. $\vec{J}_T = -\frac{NDQ}{kT^2}\nabla T$. It uses Q the heat of thermal diffusion. $\vec{J}_\sigma = \frac{ND\Omega}{kT}\nabla H$ Here $\Omega = 1 / N_0$ is the atomic volume and N_0 is initial atomic concentration, $H = (\sigma_{11} + \sigma_{22} + \sigma_{33}) / 3$ is the hydrostatic stress and $\sigma_{11}, \sigma_{22}, \sigma_{33}$ are the components of principal stress. $\vec{J}_N = -D\nabla N$.

  - Assuming a vacancy mechanism for atom diffusion we can express D as a function of the hydrostatic stress $D = D_0 \exp(\frac{\Omega H - E_A}{kT})$ where E_A is the effective activation energy of the thermal diffusion of metal atoms. The vacancy

concentration represents availability of empty lattice sites, which that might be occupied by a migrating atom.

1.1.5 Electromigration reliability of a wire (Black's equation)

- At the end of the 1960s J. R. Black developed an empirical model to estimate the MTTF (mean time to failure) of a wire, taking electromigration into consideration (as Fig 1).

$$MTTF = A(J^{-n})e^{\frac{E_a}{kT}}$$

- It is clear that current density J and (less so) the temperature T is deciding factors in the design process that affect electromigration.
- The temperature of the conductor appears in the exponent. It strongly affects the MTTF of the interconnect lines. For an interconnect lines to remain reliable in rising temperatures, the maximum tolerable current density of the conductor must necessarily decrease.

1.1.6 Wire material

- It is known that pure copper used for Cu-metallization is more electromigration-robust than aluminum. Copper wires can withstand approximately five times more current density than aluminum wires while assuming similar reliability requirements. This is mainly due to the higher electromigration activation energy levels of copper caused by its superior electrical and thermal conductivity as well as its higher melting point (as Fig.14 and Fig. 15).

Name	Aluminum
Symbol	Al
Atomic number	13
Atomic weight	26.981538
Discoverer	Hans Christian Oersted
Discovered at	Denmark
Discovery date	1825
Origin of name	From the Latin word "alumen" meaning "alum"
Density of solid	2.70 g/cm^3
Molar volume	10.00 cm^3
Velocity of sound	5100 m/sec
Hardness	2.75
Electrical resistivity	2.65 μΩ cm
Reflectivity	71%
Melting point	660 C
Boiling point	2519 C
Thermal conductivity	235 W m^{-1} K^{-1}
Coefficient of linear thermal expansion	23.1 10^{-6} K^{-1}
Etchants (wet)	H_3PO_4, HNO_4, CH_3COOH
Etchants (dry)	Cl_2, BCl_3
CVD Precursor	$Al(CH_3)_2H$

Fig. 14 The table of aluminum element.

【Hong Xiao, Introduction to semiconductor Manufacturing Technology, 2001/05/27】

Name	Copper
Symbol	Cu
Atomic number	29
Atomic weight	63.546
Discoverer	Copper had been used by human being since ancient time, long before any written history.
Discovered at	
Discovery date	
Origin of name	From the Latin word "cuprum" meaning the island of "Cyprus"
Density of solid	8.92 g/cm^3
Molar volume	7.11 cm^3
Velocity of sound	3570 m/sec
Hardness	3.0
Reflectivity	90%
Electrical resistivity	1.7 μΩ·cm
Melting point	1084.77 °C
Boiling point	5555 °C
Thermal conductivity	400 W m^{-1} K^{-1}
Coefficient of linear thermal expansion	16.5×10^{-6} K^{-1}
Etchants (wet)	HNO_4, HCl, H_2SO_4
Etchants (dry)	Cl_2, needs low pressure and high temperature
CVD Precursor	(hfac)Cu(tmvs)

Fig. 15 The table of copper element.

【Hong Xiao, Introduction to semiconductor Manufacturing Technology, 2001/05/27】

1.1.7 Summary

Electromigration is generally considered to the result of momentum transfer from the electrons, and it move in the applied electric field, to the ions which make up the lattice of the interconnect material.

Now semiconducting chips include a dense array of narrow, thin-film metallic conductors that serve to transport current between the difference devises on the chip. These metallic conductors are called interconnects.

As ICs become progressively more complex, the individual components must become increasingly more reliable if the reliability of the whole is to be acceptable. Anyway, due to continuing miniaturization of very large scale integrated (VLSI) circuits, thin-film metallic conductors or interconnects are subject to increasingly high current densities. Under these conditions, the electromigration can induce to the electrical failure of interconnects in relatively short times, reducing the circuit lifetime to an unacceptable level. It is therefore of great technological importance to understand and control electromigration failure in thin film interconnects.

In conventional metal wires like those used in house wiring, joule heating limits the allowable current to about 105 $A.cm^{-2}$. At current densities higher than this the wire will heat up and fuse. Because they are deposited onto large efficient single crystal silicon heat sinks, thin film interconnects in ICs can sustain current densities up to 1012 $A.cm^{-2}$ without immediate damage.

The electromigration causes several different kinds of failure in narrow interconnect. The most familiar are void failures along the length of the line and diffusive displacements at the terminals of the line that destroy electrical contact. The research has shown that both of these failure modes are strongly affected by the microstructure of the line and can, therefore be delayed or overcome by metallurgical changes that alter the microstructure (as Fig. 16).

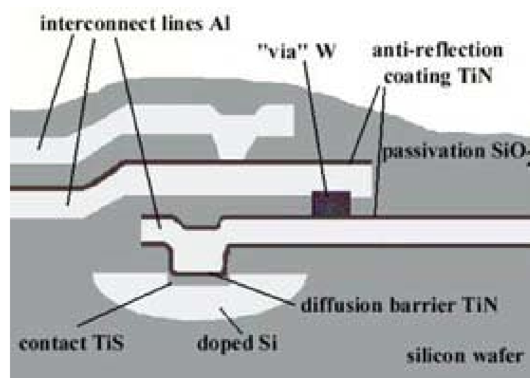


Fig. 16 A cross-sectional view of the interconnect structure.

【http://www.csl.mete.metu.edu.tr/Electromigration/emig.htm】

When electrons are conducted through a metal and they interact with imperfections in the lattice and scatter. Scattering occurs whenever an atom is out of place for any reason. Thermal energy produces scattering by causing atoms to vibrate. This is the source of resistance of metals. The higher the temperature, the more out of place the atom is the scattering and the greater the resistivity.

For the electromigration we need a lot of electrons, and also we need electron scattering electromigration does not occur in semiconductors microstructure, but it may in some semiconductor materials if they are so heavily doped that they exhibit metallic conduction.

1.2 Application

1.2.1 Line effect

- The electromigration is the momentum of atoms in response to “the electron wind”. The momentum transfer with the electrons pushing the atoms.
- It can induce to circuit failure through metal lines resistance increase or in the extreme the line opens (as Fig. 17).

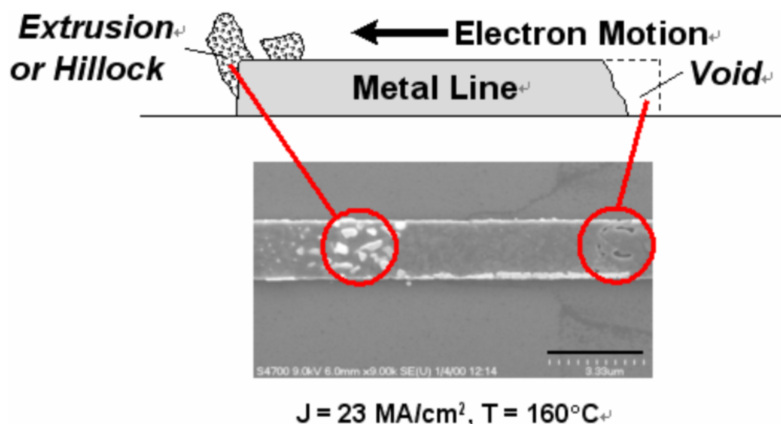


Fig. 17 The electromigration induced the line effect.

【Image courtesy of T. Alford, Arizona State University】

- The momentum of atoms dominated by changes in mobility, e.g., at grain boundaries lattice (as Fig. 18).
- The collision of electrons with atoms momentum transfer.

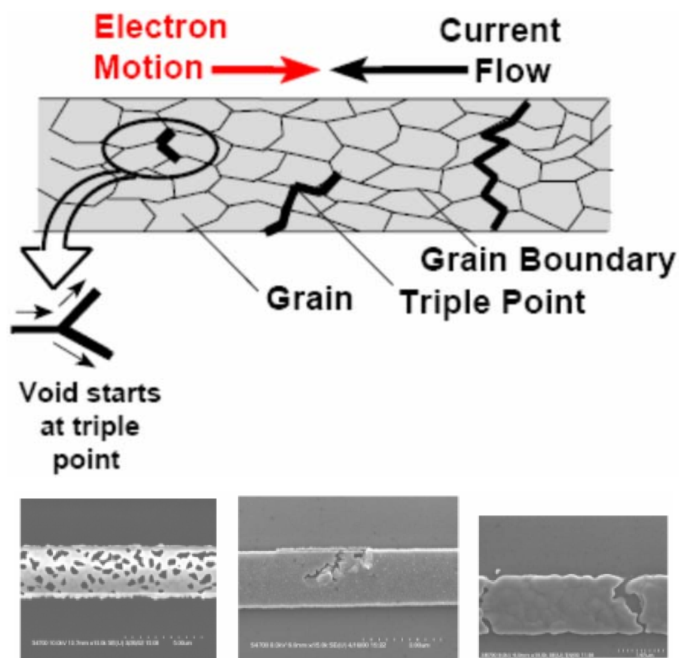


Fig. 18 The electromigration effect at grain boundary.

【Micrographs courtesy of K. Gadre and P. Nguyen, Arizona State University】

1.2.2 Passivating layers (As Fig. 19)

- The stress develops by migrating atoms.
- The passivating layers contain the stress, but cracks in such layers enhance electromigration effect.

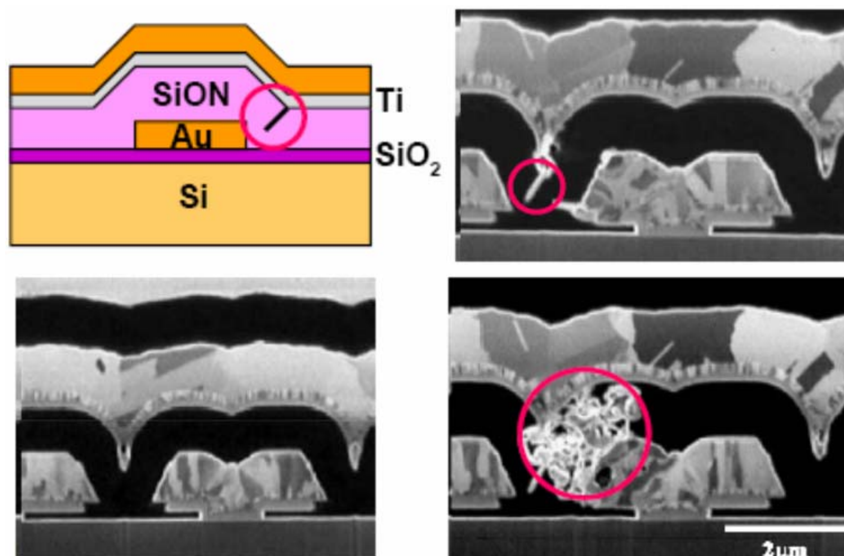


Fig. 19 The electromigration effect at passivating layers.

【H. Murayama et al., Microelectron. Rel. 41, 1265 (2001)】

1.2.3 Via issue (as Fing.20 and Fig.21)

- Contact or via of electromigration can occur due to high current densities:
  - Poor metal step coverage.
  - Different materials, e.g., W plugs/Al lines.
  - Al electromigration is not re-supplied by W (no voids for Al plugs).
- Contact (Via) electromigration:
  - The current continues to flow through the Ti/TiN and Al_3Ti layers when there is a void, but the resistance increases.

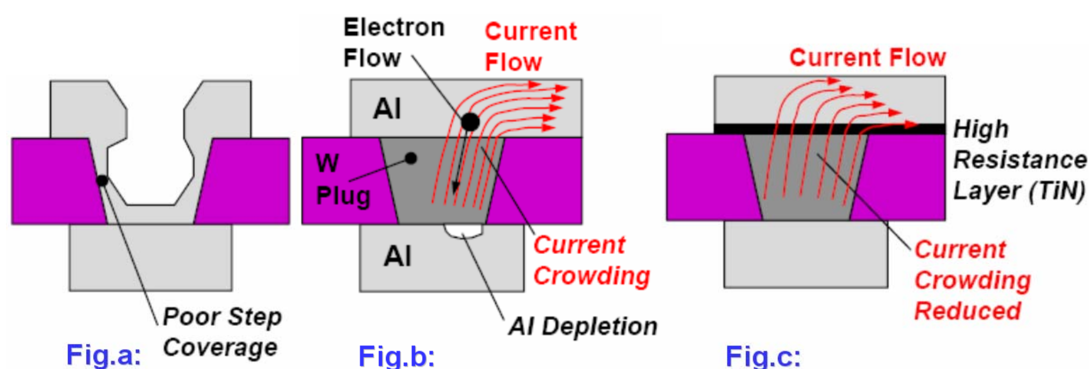


Fig. 20 The electromigration effect at via issue.

【Image courtesy of T. Alford, Arizona State University】

Fig. a If there are poor step coverage, it would has a void at the via.

Fig. b If W plug don’t cover the TiN, it will has current crowding effect (high current density at corner).

Fig. c The TiN layer likes a filter, and it can reduce current crowding effect.

Remark:

TiN:

- The resistivity of TiN is high than W and Al.
- It can reduce the contact resistance (Glue layer).
- Barrier layer.

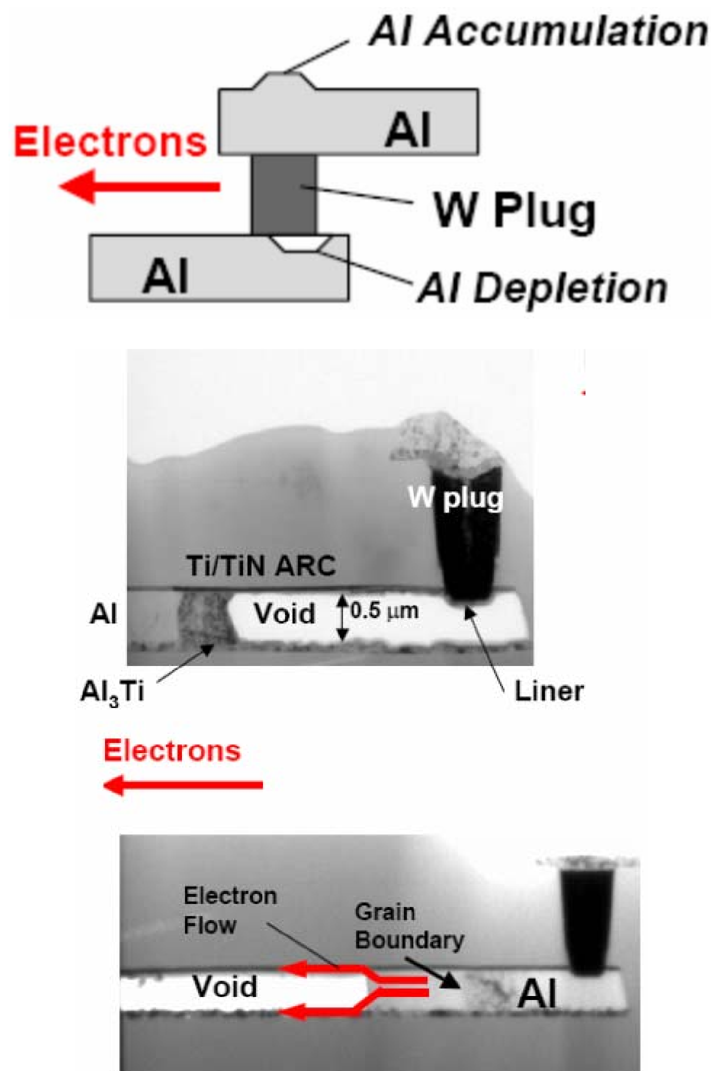


Fig. 21 The electromigration effect at via.

【TEM Micrographs Courtesy of T.S. Sriram and E. Piccioli, Compaq Computer Corporation】

- Via electromigration test structure:
  - The force current through via.
  - To change current direction allows upper and lower interfaces to be probed.
  - Can combine with poly-Si resistance heater to change temperature.

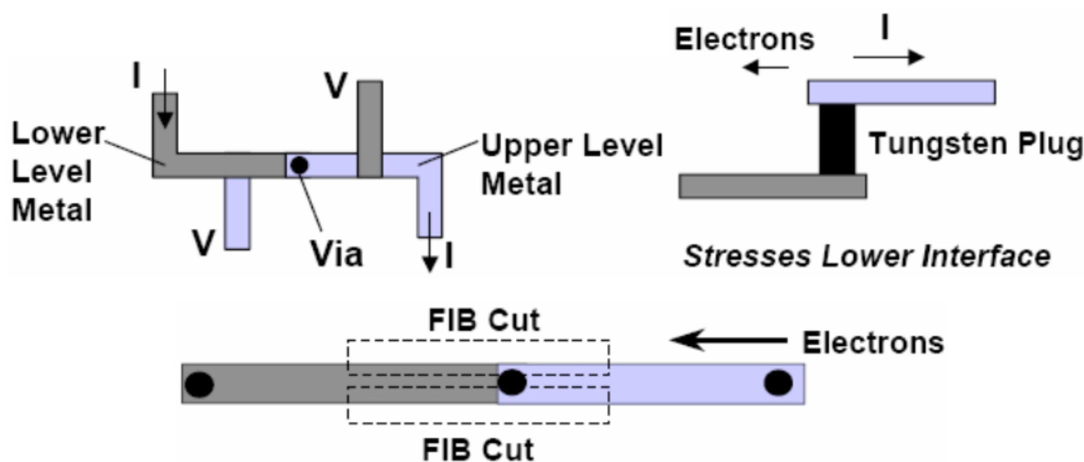


Fig. 22 via electromigration test structure.

【Image courtesy of T. Alford, Arizona State University】

1.2.4 EM in Solder Joints for flip-chip

- For solder joints used in IC chips, the atoms pile up at the anode, voids are generated at the cathode and back stress is induced during electromigration. The typical failure of a solder joint due to electromigration will occur at the cathode side. Due to the current crowding effect, voids form at the corner of the solder joint first. Then the voids extend and cause a failed circuit (as Fig. 23).

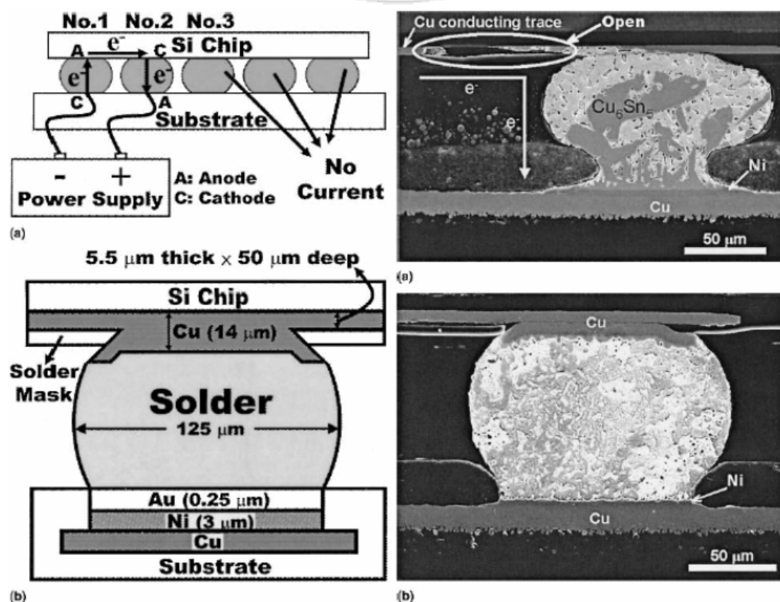


Fig. 23 The electromigration in solder joints for flip-chip.

【Y.C. Hu, Y.H. Lin, and C.R. Kao, Electromigration failure in flip chip solder joints due to rapid dissolution of copper, 2003/08/22】

1.3 Conclusion

1.3.1 What is EM (electromigration)?

- The mass transport of a metal due to the momentum transfer between conducting electrons and diffusing metal atoms, this is exists current flows through metal wires.
- The conditions necessary for electromigration to be a significant problem continue to bear down on us with increasing speed and ferocity:
  - High current densities.
  - Long narrow wires.
  - Logic hazards.
  - High operating frequencies.
- The microstructure of the metallization induces to the atomic flow being non-uniform, and damage results in the form of voids or hillocks.
- The temperature and electron wind force are main factor for electromigration.

1.3.2 How to improve electromigration issue in future?

- The Cu has been used as a common alloy metal (typically between 0.5wt-% and 3wt-%) in aluminum interconnects to improve electromigration resistance and reliability.
- An optimized coarse-grained switching cell is designed to prevent electromigration, minimize voltage drop, and ensure fast wake-up time.
- Passivation openings should be designed to be as large as possible to reduce current density and improve electromigration life times.
- To reduce the operation voltage and temperature.
- Raising adhesion strength between metal and metal alloy.
- To form good step coverage at via.
- New solder material be improved the EM effect.

Chapter 2 Strain Technology

2.1 Abstract

The strained channel technology has been examined over twice decades because it enhances the carrier mobility contributing to the device drive current. Recently it has proposed to be integrated into integrated circuit industry for the CMOS higher performance. Although there are many methods to seek for higher device performance enhancement, but the strain technology is the promising candidate. In this chapter we will focus on the strained silicon channel on general (100) silicon wafer. We will discuss the fundamentals of strained silicon physic mechanism, the recent proposed technology and the future work.

2.2 Introduction

Silicon CMOS has emerged over the last 25 years as the predominant technology of the microelectronics industry. The concept of scaling has been consistently applied over many technology generations, resulting in consistent improvement in both device density and performance. Device dimensions are shrunk from the micrometer scale into the nanometer regime. Scaling of MOSFET is continuing for higher device performance, higher integrated circuit density, lower cost and etc. According to design rule, when the dimension of device is scaled down, the silicon dioxide thickness must be scaled down. Because of the short channel effects, the junction depth must be shallower, the substrate impurity concentration must be higher etc. Device performance can improve by inducing a larger charge density for a given gate voltage drive; enhancing the carrier transport; ensuring device scalability to achieve a shorter channel length; and reducing parasitic capacitances and parasitic resistances. Fig. 24 summarizes these opportunities/challenges and corresponding proposed technology options. These options can be classified into two categories: new materials and new device structures, which are usually related. As summarized in the table below, strained silicon could be one of the candidates to enhance the carrier transport. A high dielectric constant (κ) material is required to achieve low equivalent oxide thickness (EOT). When the requirements of device performance or reliability can't be reached, we must

change the material or structure. For example we replace silicon dioxide by the high-k material when the thickness of silicon dioxide is thinner than 2 nanometer. It suffers from carrier directly tunneling. Although using the high – k dielectric have a thicker physic thickness preventing from carrier directly tunneling, but it also leads to the degradation of mobility due to the uncertain or additional scattering mechanism. If we want to continue the Moore's law, the use of high-k dielectric is necessary but we don't want the mobility to degrade due to the introduction of high-k dielectric. Strained channel technology can overcome this disadvantage. In 2002 IEDM, Intel publishes the introduction of strain. Recently the International Technology Roadmap for semiconductor recognized that local strain has been integrated into current IC manufacturing and should be extendable to at least the 32 nm generation in Fig. 25 and Fig. 26.

Source of improvement	Parameters affected	Method
Charge density	• S (inverse subthreshold slope) • Q_{inv} at a fixed I_{off}	1. Double-gate FET. 2. Lowered operating temperature.
Carrier transport	• Mobility (μ_{eff}) • Carrier velocity • Ballistic transport	1. Strained silicon. 2. High-mobility and saturation-velocity materials (e.g., Ge, InGaAs, InP). 3. Reduce mobility degradation factors (e.g., reduced transverse electric field, reduced Coulomb scattering due to dopants, reduced phonon scattering). 4. Shorter channel length. 5. Lowered operating temperature.
Parasitic resistance	• R_{ext}	1. Extended/raised source/drain. 2. Low-barrier Schottky contact.
Parasitic capacitance	• C_{jn} • C_{GD}, C_{GS}, C_{GB}	1. SOI. 2. Double-gate FET.
Ensuring device scalability to a shorter channel length	• Generalized scale length (λ) • Channel length (L_g)	1. Maintaining good electrostatic control of channel potential (e.g., double-gate FET, ground-plane FET, and ultrathin-body SOI) by controlling the device physical geometry and providing means to terminate drain electric fields. 2. Sharp doping profiles, halo/pocket implants. 3. High gate capacitance (thin gate dielectrics, metal gate electrode) to provide strong gate control of channel potential.

Fig. 24 Potential solutions to improve device performance

【H. S. P. Wong, "Beyond the conventional transistor," IBM Journal of Research and Development, vol. 46, pp. 133-168, 2002.2】

Front End Processes Difficult Challenges—Near-term Years

Difficult Challenges ≥ 32 nm	*Summary of Issues*
New gate stack processes and materials	Extension of oxynitride gate dielectric materials to $<$ 1.0 nm EOT for high-performance MOSFETs, consistent with device reliability requirements
	Control of boron penetration from doped polysilicon gate electrodes while minimizing depletion of dual-doped polysilicon electrodes
	Introduction and process integration of high-κ gate stack materials and processes for high-performance, low operating and low standby power MOSFETs
	CMOS integration of enhanced channel mobility in both NMOS and PMOS devices, using local and global strained layers
	Introduction of dual metal gate electrodes with appropriate work function
	Control of silicon loss at spacer etch and gate etch needs to be much tighter on thin SOI and SiGe wafers, where the total silicon thickness is 20–50 nm
	Removal of high-κ dielectric without loss of the underlying silicon, especially in the case of SOI or non planar devices
	Metrology issues associated with gate dielectric film thickness and gate stack electrical and materials characterization
Critical dimension and effective channel length (L_{eff}) control	Control of gate etch processes that yield a physical gate length that is considerably smaller than the feature size printed in the resist, while maintaining $<$12% overall 3-sigma control of the combined lithography and etch processes
	Control of profile shape, edge roughness, line and space width for isolated as well as closely-spaced fine line patterns
	Control of self-aligned doping processes and thermal activation budgets to achieve L_{eff} control
	Maintenance of CD and profile control throughout the transition to new gate stack materials and processes
	CD and etch metrology
	Site flatness to ensure effective lithographic printing
Introduction and CMOS integration of new memory materials and processes	Development and introduction of very high-κ DRAM capacitor dielectric layers
	Migration of DRAM capacitor structures from silicon-insulator-metal to metal-insulator-metal
	Integration and scaling of FeRAM ferroelectric materials
	Scaling of Flash interpoly and tunnel dielectric layers may require high-κ
	Limited temperature stability of high-κ and ferroelectric materials challenges
	CMOS Integration
Surfaces and interfaces—structure, composition, and contamination control	Contamination, composition, and structure control of channel/gate dielectric interface as well as gate dielectric/gate electrode interface
	Interface control for DRAM capacitor structures
	Maintenance of surface and interface integrity through full-flow CMOS processing
	Statistically significant characterization of surfaces having extremely low defect concentrations for starting materials and pre-gate clean surfaces
	Measurement of back surface particles at/near edge wafer edge (including bevel) has no solution
	Measurement and understanding of clustering of particles needs significant data to define future specification
	Little information associating back surface particles and the effect on yield
Scaled MOSFET dopant introduction and control	Doping and activation processes to achieve shallow source/drain regions having parasitic resistance that is less than ~17–33% of ideal channel resistance ($=V_{dd}/I_{on}$)
	Control of parasitic capacitance to achieve less than ~23–29% of gate capacitance, consistent with acceptable Ion and minimum short channel effect
	Achievement of activated dopant concentration greater than solid solubility in dual-doped polysilicon gate electrodes
	Formation of continuous self-aligned silicide contacts over shallow source and drain regions. Formation of elevated junctions and silicides on FDSOI wafers
	Metrology issues associated with 2D dopant profiling

Fig. 25 ITRS 2005

【2005 International Technology Roadmap for Semiconductor】

DIFFICULT CHALLENGES

Front End Processes Difficult Challenges—Near-term Years UPDATED

Difficult Challenges ≥ 32 nm	*Summary of Issues*
New gate stack processes and materials	Extension of oxynitride gate dielectric materials to < 1.0 nm EOT for high-performance MOSFETs, consistent with device reliability requirements Control of boron penetration from doped polysilicon gate electrodes while minimizing depletion of dual-doped polysilicon electrodes Introduction and process integration of high-κ gate dielectrics ~~stack materials~~ and processes for high-performance, low operating ~~and low standby~~ power MOSFETs ~~CMOS integration of enhanced channel mobility in both NMOS and PMOS devices, using local and global strained layers~~ Introduction of dual metal gate electrodes with appropriate work function Control of silicon loss at spacer etch and gate etch needs to be much tighter on thin SOI and SiGe wafers, where the total silicon thickness is 20–30 nm Removal of high-κ dielectric without loss of the underlying silicon, especially in the case of SOI or non planar devices Metrology issues associated with gate dielectric film thickness and gate stack electrical and materials characterization
Critical dimension and effective channel length (L_{eff}) control	Control of gate etch processes that yield a physical gate length that is considerably smaller than the feature size printed in the resist, while maintaining <12% overall 3-sigma control of the combined lithography and etch processes Control of profile shape, edge roughness, line and space width for isolated as well as closely-spaced fine line patterns Control of self-aligned doping processes and thermal activation budgets to achieve L_{eff} control Maintenance of CD and profile control throughout the transition to new gate stack materials and processes CD and etch metrology Site flatness to ensure effective lithographic printing
Introduction and CMOS integration of new memory materials and processes	Development and introduction of very high-κ DRAM capacitor dielectric layers Migration of DRAM capacitor structures from silicon-insulator-metal to metal-insulator-metal Integration and scaling of FeRAM ferroelectric materials Scaling of Flash interpoly and tunnel dielectric layers may require high-κ Limited temperature stability of high-κ and ferroelectric materials challenges CMOS Integration
Surfaces and interfaces—structure, composition, and contamination control	Contamination, composition, and structure control of channel/gate dielectric interface as well as gate dielectric/gate electrode interface Interface control for DRAM capacitor structures Maintenance of surface and interface integrity through full-flow CMOS processing Statistically significant characterization of surfaces having extremely low defect concentrations for starting materials and pre-gate clean surfaces Measurement of back surface particles at/near edge wafer edge (including bevel) has no solution Measurement and understanding of clustering of particles needs significant data to define future specification Little information associating back surface particles and the effect on yield
Scaled MOSFET dopant introduction and control	Doping and activation processes to achieve shallow source/drain regions having parasitic resistance that is less than ~17–33% of ideal channel resistance (=V_{dd}/I_{on}) Control of parasitic capacitance to achieve less than ~23–29% of gate capacitance, consistent with acceptable Ion and minimum short channel effect Achievement of activated dopant concentration greater than solid solubility in dual-doped polysilicon gate electrodes Formation of continuous self-aligned silicide contacts over shallow source and drain regions. Formation of elevated junctions and silicides on FDSOI wafers Metrology issues associated with 2D dopant profiling

Fig. 26 ITRS 2006 update

【2006 update International Technology Roadmap for Semiconductor】

2.3 Physic mechanism

Now we will start to discuss the physic mechanism about strained silicon channel. In this section all we discuss is the conventional (100) silicon wafer. This is because the different growth orientation wafer has different responses of different kinds of strain due to lattice structure leading to different band structure (e.g. Fig. 27) then if we consider above, it will become more complex. Hereby in this section we just only simply discuss the conventional (100) silicon wafer.

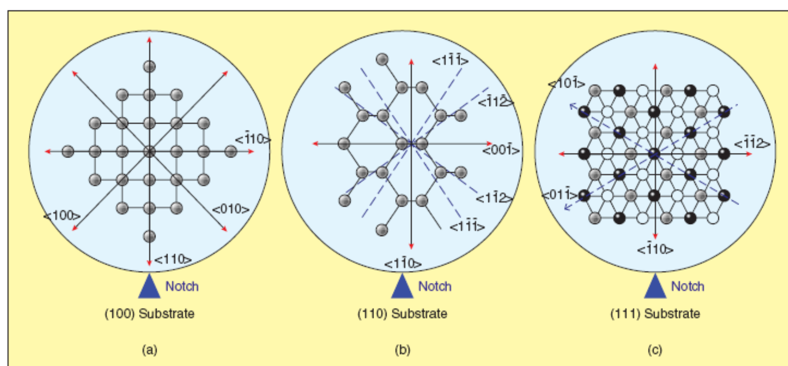


Fig. 27 The different channel orientations on (a) (100) substrate, (b) (110) substrate, and (c) (111) substrate.

【Mobility-enhancement technologies，Chee Wee Liu, S. Maikap, and C.-Y. Yu，IEEE CIRCUITS & DEVICES MAGAZINE MAY/JUNE 2005】

In Fig. 28 we know when we shrink the device dimension; the applied voltage can’t be shrunk like it. Because of maintaining the sufficient drive current. As a resulting, the vertical field will increases with the dimension scaling down. The increasing vertical field degrades the mobility due to the different scattering mechanism. The reader is referred elsewhere for further discussion of mobility in Si inversion layers.

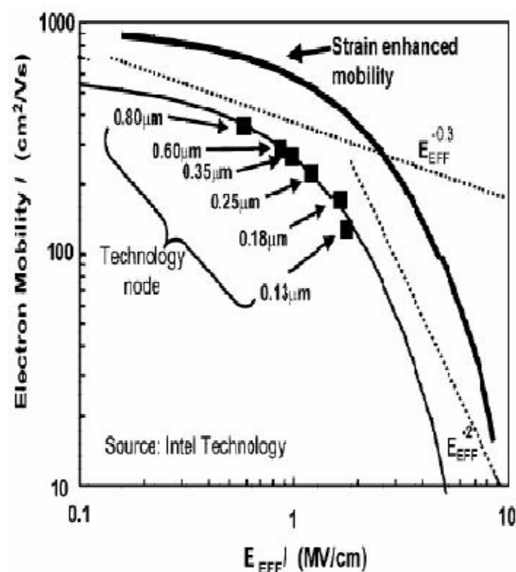


Fig. 28 Mobility degrades with increasing the vertical field.

【S.Thompson etc. A 90 nm logic technology featuring 50 nm strained silicon channel transistors, 7 layers of Cu interconnects, low k ILD, 2002 IEDM pp61-64】

Therefore, for the higher drive current we must enhance the carrier mobility. Hereby there two approaches are used for enhancing mobility.

1. Strain technology.
2. Size effect.

Below we will discuss them respectively.

There are many methods used for the strained-channel by the naturally different lattice constant, partial process steps or device packaged. In this section we will introduce the substrate-based strain (biaxial train) and process-based strain (uniaxial strain).

- Biaxial strain:

  Biaxial strain is also referred as global strain; it is substrate-based strain technology.

  The strain exists in the surface parallel to substrate and vertical channel. The schematics Fig. 29 illustrate the structure.

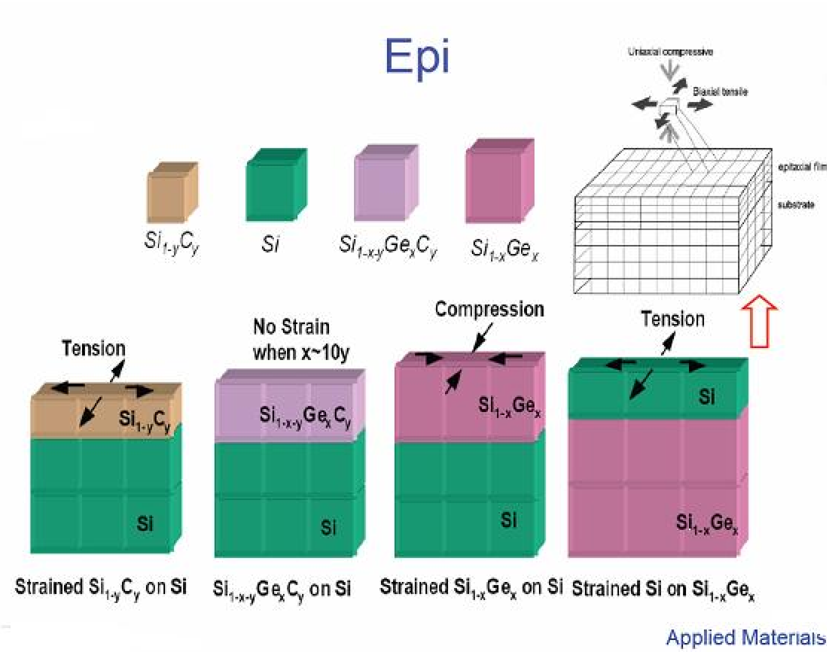
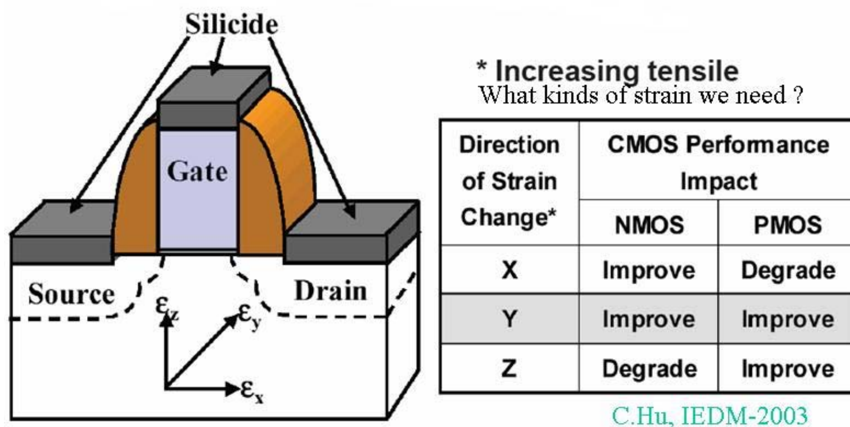


Fig. 29 Biaxial strain illustration.

【Applied Materials】

Under the biaxial strain, there is the same strain in the different position. Biaxial tensile stress could improve both N(electron mobility) and P(hole mobility) -MOSFETs simultaneously. Although, this is true, it occurs only at low electric field and high stress Because of PMOS degrades at high electric field. (I.e. Fig. 30), and we will discuss this phenomena later.



Direction of Strain Change*	CMOS Performance Impact	
	NMOS	PMOS
X	Improve	Degrade
Y	Improve	Improve
Z	Degrade	Improve

Fig. 30 Biaxial strain illustration

【C.Hu, IEDM-2003】

- Uniaxial strain:

  Uniaxial strain is also referred as local strain. There is different strain in different position. And it is relative to device structure, channel length and channel width. The Fig. 30 illustrates the uniaxial strain, and points out what kinds of strain we need.

- Effect of strain on mobility

  In Fig. 28 we know the mobility is limited by impurity scattering, phonon scattering and surface roughness scattering. Therefore the performance gain is possibly resulting from light effective mass, reduced inter-valley scattering and having a better heterointerface than that between silicon and silicon dioxide.

  Considering the constant energy surface of silicon (100) conduction band in Fig. 31.

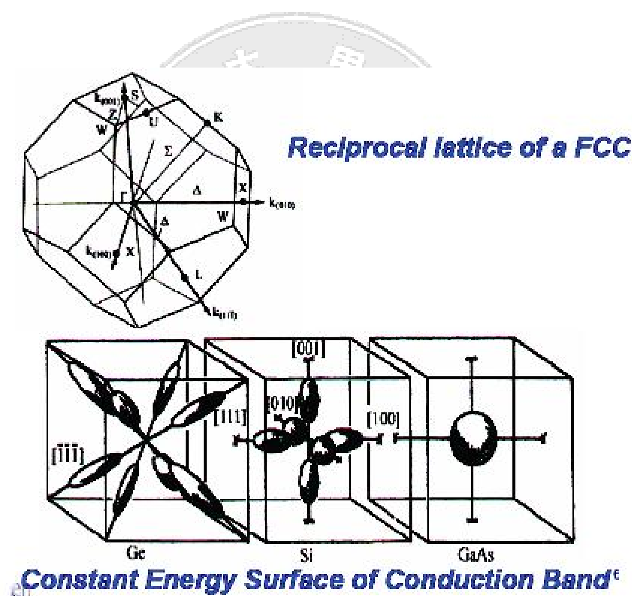


Fig. 31 Constant energy surface of conduction band illustration

【S.M.Sze, Semiconductor Device Development in the 1970s and1980s – A perspective, "Proc. IEEE, 69, 1121(1981).】

The electron transport characteristic is determined by the Six-fold valley and in the equilibrium the Six-fold valley is degenerate, then the occupancy possibility of electrons in the Six-fold valley is equal.

If we consider 2-D transport plane, the 2-fold valley is the optimum electronic system as schematically shown in Fig. 32.This is because the 2-fold valleys have the lower effective mass parallel to the Si/SiO2 interface which increase mobility and the higher effective mass perpendicular to the interface

which increases inversion layer capacitance. Both of causations the occupancy of 2-fold valleys contribute to higher current drive of MOSFETs., Therefore if we increase the 2-fold valley occupancy , the electrons will transport by lighter effective mass then increase the electron mobility .The occupancy of 2-fold valleys is determined by the subband energy difference between the 2-fold valleys and 4-fold valleys. Hereby when we increase the splitting energy, the mobility will be enhanced due to increased 2-fold valleys occupancy, as schematically shown in Fig. 33. In Fig. 33 we know size effect and strain can increase the splitting energy. Fig. 34 shows when the thickness of Si channel on Insulator is between 3nm and 5nm, the mobility is increased due to the all electrons populate in 2-fold valleys-Except strain and size effect, the vertical electric field can also increase the splitting energy. And this is why the electron mobility enhancement is still maintained at high electric field! It is not only because reduced effective mass but also reduce intervalley scattering due to energy splitting. For a given strain, quantifying the effective mass reduction and comparing it to the enhanced Mobility reveals that mass reduction alone explains only part of the mobility enhancement Hence, electron scattering must also be reduced due to the conduction valleys splitting into two sets of energy levels, which lowers the rate of Inter-valley phonon scattering between the 2-fold valley and 4-fold valleys. Quantifying the improvement due to scattering has been difficult using acceptable scattering parameters, but reduced scattering is still believed to account for the rest of the mobility enhancement. Now we will discuss why the Gate voltage-induced quantum confinement (vertical field) also affects the splitting of 2-fold and 4-fold valleys. As schematically shown in Fig. 36, the vertical field affects the position of ground stares of 2-fold and 4-fold valleys is determined by the out-of-plane effective mass of 2-fold and 4-fold valley. As a resulting, the total splitting energy is equal to the strain-induced energy splitting plus the vertical field-induced energy splitting. According to this result, when the splitting energy is increased some scattering path will be suppressed. It is also contributed to the mobility enhancement.

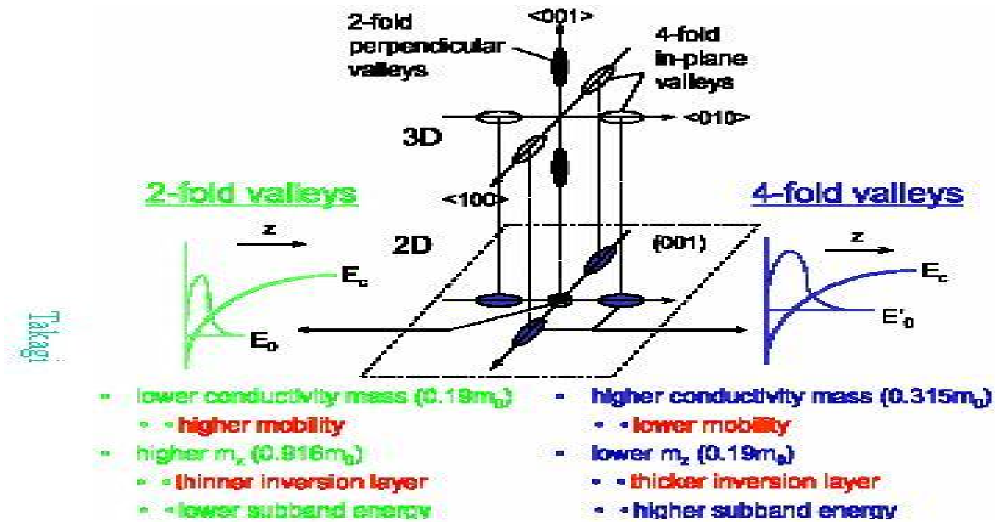
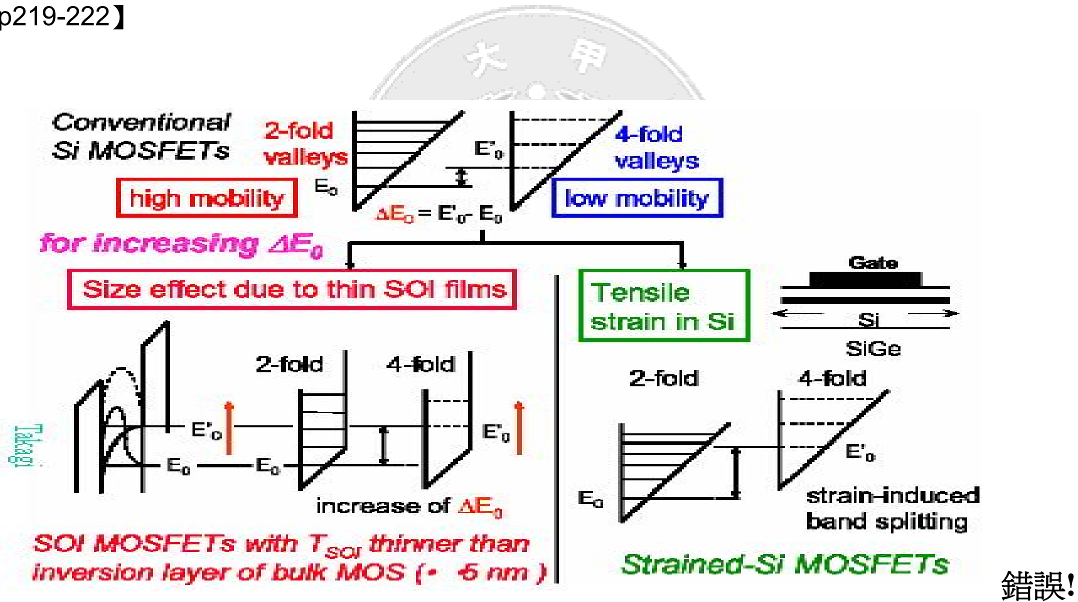


Fig. 32 Schematic subband structure of 2-D electron on (100) and the characteristics of two kinds of subbands ; the 2-fold and 4-fold valley.

【Subband structure engineering for performance enhancement of Si MOSFETs IEDM-97 pp219-222】



錯誤!

Fig. 33 Two device structure to enhance the electron occupancy of the 2-fold valleys by increasing the energy different.

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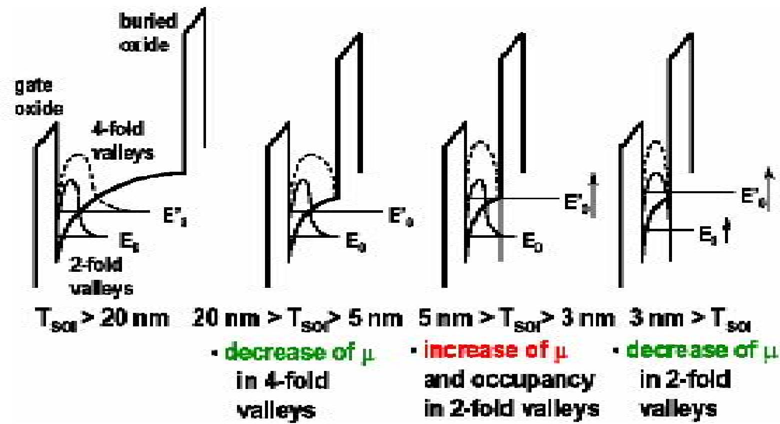

Fig. 34 Schematic diagrams of the band structure of SOI MOSFETs with different Si channel thickness

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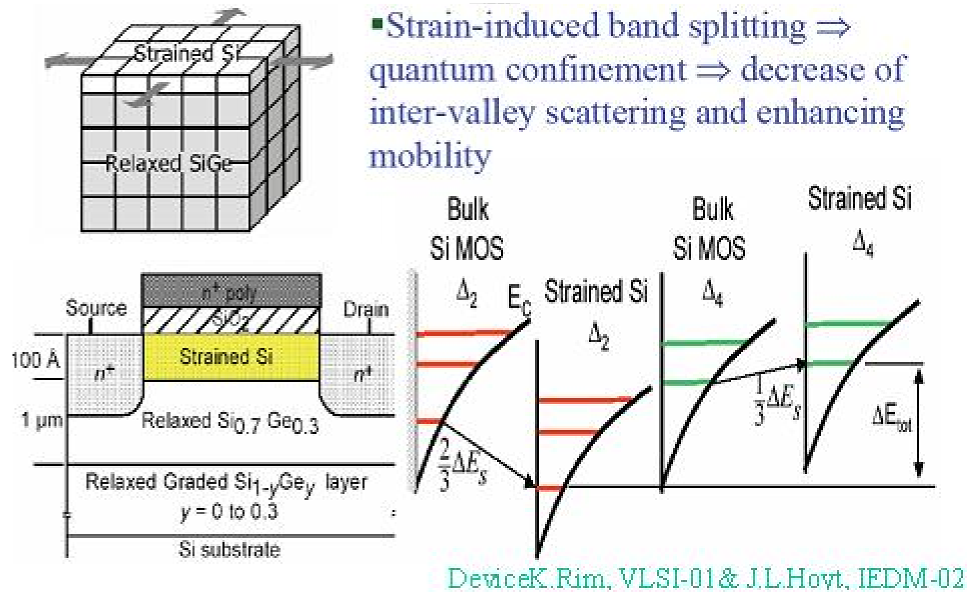

Fig. 35 Strain-induced band splitting

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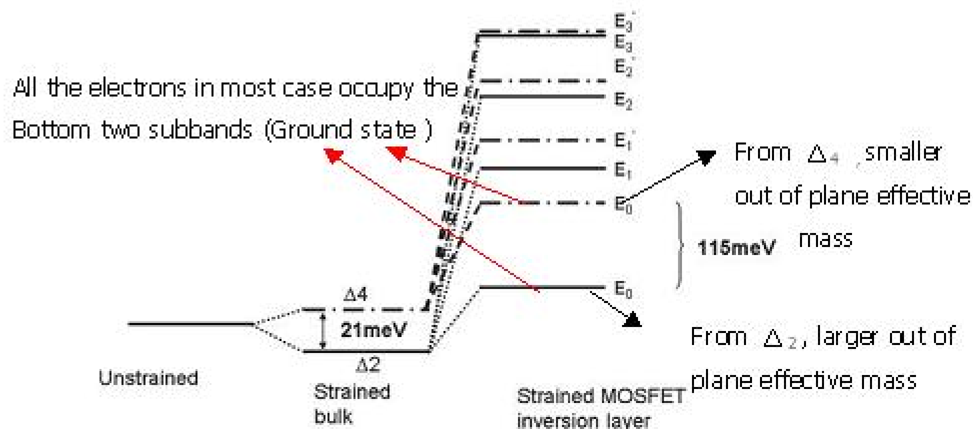


Fig. 36 Strained MOSFET inversion layer

【Mobility-enhancement technologies , Chee Wee Liu, S. Maikap, and C.-Y. Yu , IEEE CIRCUITS & DEVICES MAGAZINE MAY/JUNE 2005】

Up to now we only discuss the electron mobility enhancement under the biaxial tensile strain, the hole mobility enhancement is similar to electron, but there are something different. The electron mobility enhancement is resulting from the repopulation of electrons and reduced intervalley scattering. The hole mobility enhancement mainly is resulting from the reduced effective mass due to strain-induced valence band warping, As schematically shown in Fig. 37, hole constant-energy band surfaces for the top band obtained from six-band k • p calculations for common types of 1-GPa stresses: (a) unstressed (b) biaxial tension, (c) longitudinal compression on (001) wafer, and (d) longitudinal compression on (110) wafer (note significant differences in stress induced band warping altering the effective mass). By comparing the figure 11(a) and (b) we can understand why the holes mobility degrades at high field under biaxial tensile. This is because of the different out-of-plane effective mass between top band and second band (here the top band and second band differ from the light-hole band and heavy-hole band, because the light-hole band and heavy-hole band lose their meaning). This situation is opposite to the electron , because the splitting energy between top and second bands is decreased by vertical field increasing interband scattering , as schematically shown in Fig 38.

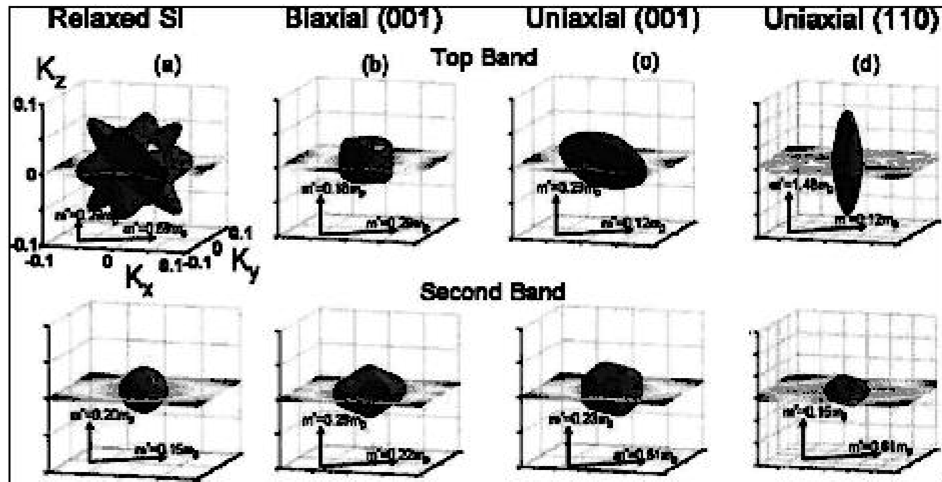


Fig. 37 Lattice classify

【S.M.Sze, Semiconductor Device Development in the 1970s and1980s – A perspective, "Proc. IEEE, 69, 1121(1981).】

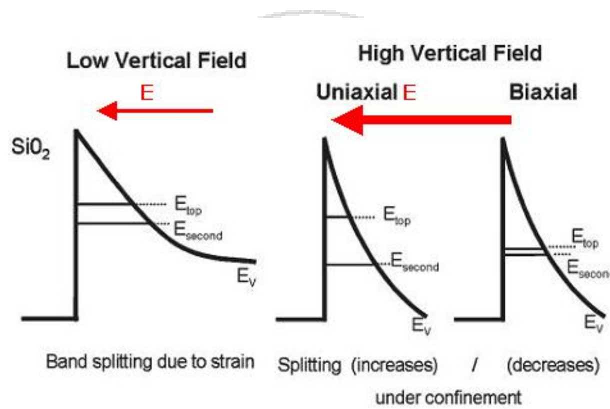


Fig. 38 Vertical field

【S.Thompson etc Uniaxial-process-induced strained-Si extending the CMOS roadmap ,E.D, vol.53,pp1010】

2.4 Recent technology

In this section we will introduce several proposed strain technologies.

- Substrate-based strained-Si channel MOSFET:

  The strained-Si channel is grown on relaxed SiGe layer /or graded SiGe layer, in which there are misfit dislocation formed due to the strain relaxation. So if we want to maintain strain in the Si channel, several conditions must be satisfied. The thickness of Si channel must be thinner than a critical thickness, which is a function of Ge concentration. The thickness of Si channel decreases with increasing the Ge concentration.

The thermal budget must be lowered in order to prevent the strain from relaxing and prevent Ge atoms from diffusing to the interface between gate dielectric and Si-channel, as schematically shown in Fig. 39 because the present of Ge atoms cause additional challenges the thermal instability, parasitic hole channel at the Si/SiGe interface and lower thermal conductivity of SiGe etc. All of these are need to solve.

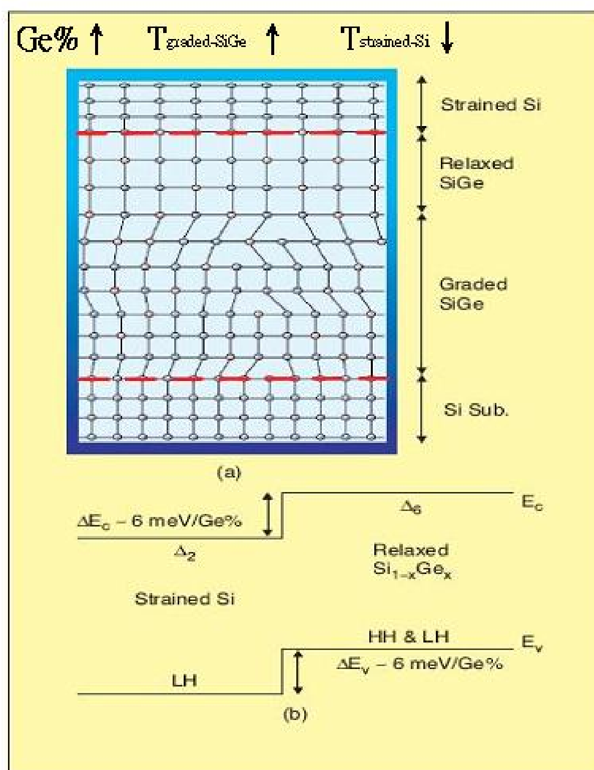


Fig. 39 Vertical field

【S.Thompson etc Uniaxial-process-induced strained-Si extending the CMOS roadmap ,E.D, vol.53,pp1010】

- Process-based strained-Si channel MOSFET:

There are several method proposed to introduce the strain in Si channel, as schematically shown in Fig. 40. According to Fig. 30 we know that there are different strain requirement for PMOS and NMOS respectively. We utilize the stop-etch-capping-layer to introduce the tensile strain and compressive strain to NMOS and PMOS by depositing LPCVD nitride layer and PECVD nitride layer respectively in Fig. 40 (a). We also utilize the different thermal expansion coefficient between silicon and silicide to introduce the strain in Fig. 40 (b). STI is frequently used for lateral isolation in deep sub-micrometer technology in Fig. 40 (C).

And the strained PMOS transistor features an epitaxially grown strained SiGe film embedded in the S/D regions using a selective epitaxial growth was reported by Intel in Fig. 40 (d).

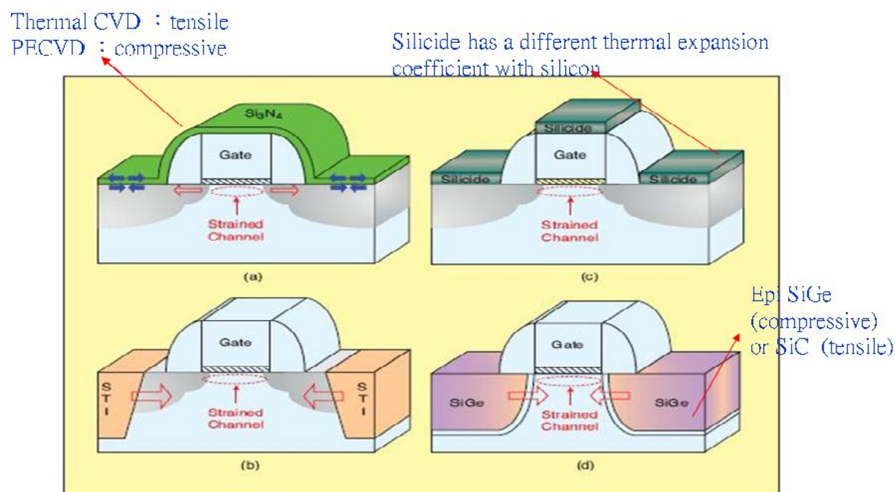


Fig. 40 there is several methods proposed to introduce the strain in Si channel, as schematically.

【S.Thompson etc Uniaxial-process-induced strained-Si extending the CMOS roadmap ,E.D, vol.53,pp1010】

2.5 Conclusion

Whether biaxial or uniaxial technologies the Future work is to integrate strain technology with high-K dielectric, Ni silicide, SOI and other advanced technology for further improving devices performance.

Chapter 3 Ni Fully Silicided (FUSI)

3.1 Abstract

A study of the implementation of Ni fully silicided (FUSI) gates to scaled devices is presented, addressing the issue of phase control at short gate lengths. A linewidth effect for Ni FUSI gates is found for non-optimized processes targeting NiSi, with formation of NiSi at long gate lengths and Ni-rich silicides at short gate lengths. This is attributed to Ni diffusion from areas surrounding the gates, resulting in a larger reacted Ni–Si ratio at short gate lengths. The linewidth dependence of the Ni FUSI phase results in an undesirable kink in the Vt roll-off characteristics, due to the difference in effective work function between the Ni silicide phases, which is particularly large for HfSiON dielectrics. An optimized 2-step RTP silicidation process is shown to eliminate this problem allowing the formation of NiSi gates uniformly at all gate lengths. The application and scalability of Ni-rich silicides to PMOS devices is also demonstrated, as well as a scheme for CMOS integration of dual WF phase controlled FUSI (NiSi for NMOS and Ni-rich silicides for PMOS), using an etch back step to reduce the poly-Si height on PMOS electrodes before full silicidation.

3.2 Introduction

Ni fully silicided (FUSI) gates are considered as candidates for metal gate electrode applications in next generation CMOS technologies. While initial work focused on NiSi FUSI gates and the modulation of its effective work function (WF) on SiO2 or SiON with dopants or alloying elements, recent work has shifted to consider other Ni silicide phases as well. On HfSiON dielectrics, there is a strong dependence of the effective WF on the Ni silicide phase, while a milder dependence on Ni silicide phase is observed for SiO2. The implications for device applications are twofold: on one hand it may be possible to take advantage of the phase dependent WF to tune transistor threshold voltages (Vt) for NMOS and PMOS devices by targeting different Ni silicide phases on NMOS and PMOS. On the other hand, the sensitivity of WF and Vt to silicide phase places a great concern on the ability to control the silicide phase in contact with the dielectric, uniformly at all gate lengths in all

transistors of a microchip. This paper addresses the implementation of Ni FUSI gates to scaled devices and the phase control issues associated with it. A linewidth effect for FUSI gates is explained in terms of the Ni–Si reaction and phase formation, suggesting the formation of NiSi gates (NiSi in contact with the dielectric) at long gate lengths and Ni-rich FUSI gates (Ni-rich silicide in contact with the dielectric) at short gate lengths for non-optimized processes targeting NiSi. The scalability of NiSi FUSI gates is demonstrated, using an optimized 2-step RTP process that results in uniform formation of NiSi gates at all gate lengths studied. The application and scalability of Ni-rich silicides to PMOS devices is demonstrated. A CMOS integration scheme for dual WF phase controlled FUSI (NiSi for NMOS and Ni-rich silicides for PMOS) is also demonstrated.

Gate depletion and boron penetration are notorious process hazards for submicron CMOS processes with their very thin gate oxides, dual flavored poly-Si and low temperature budgets. The thermal budget must be sufficient to achieve adequate gate activation to avoid performance loss caused by gate depletion. On the other hand, the temperature budget must be reduced to limit short-channel effects, as well as to avoid PMOST threshold voltage reduction due to boron penetration. This paper shows that transistor matching degrades strongly when gate depletion or boron penetration occurs. This means that these effects must be interpreted as stochastic effects, associated with the grain size distribution in the poly-Si gate and how the dopant diffuses in the gate and through gate dielectric (Fig. 41).

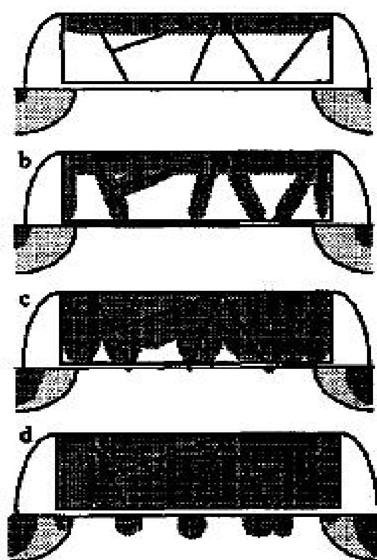


Fig. 41. Schematic representation of poly-Si grain doping stages

a: after implant, b: fast diffusion along grain boundaries, c: almost fully doped, d: local boron penetration.

3.3 NiSi salicide technology

3.3.1 Optimum silicidation temperature

Fig. 42 shows a typical salicide process for advanced CMOS. Because self-aligned silicidation is carried out after source drain formation, the silicidation temperature is desirable to be sufficiently low in order to keep ultra-shallowness of the junction for sub-100 nm technology node CMOS. Fig.44 shows a comparison of the silicidation temperature and other properties of various silicide materials. NiSi has the lowest silicidation temperature among the materials listed in the table and wide range of 350–750℃. Fig. 43 shows sheet resistance dependence on silicidation temperature for NiSi and $TiSi_2$. In the case of $TiSi_2$, the range is actually very small. The sheet resistance of TiSi2 is high below 800℃, because content of C49 crystal (higher resistivity crystal) structure increases. Between 850℃ and 950℃, the sheet resistance goes through a minimum because the phase becomes C54 structure (lower resistivity crystal). Above 950 ℃ , it becomes again higher because agglomeration of the silicide film occurs. On the other hand, the sheet resistance of NiSi is stable and minimum between 450℃ and 750℃. Increase of the sheet resistance above 800c is due to phase transition from NiSi to $NiSi_2$. Thus, NiSi is the most suitable from the viewpoint of low process temperature for sub-100-nm technology node (or sub-50-nm gate length) CMOS. On the other hand, it should be noted that the process temperature after the salicide should not be higher than 750℃.

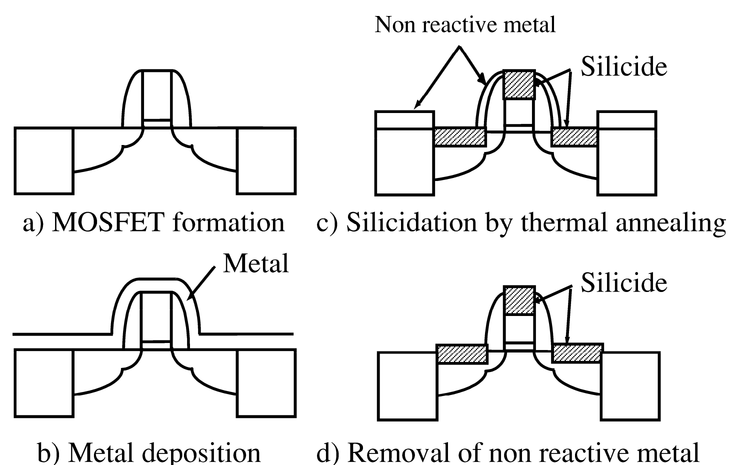


Fig.42. A typical salicide process.

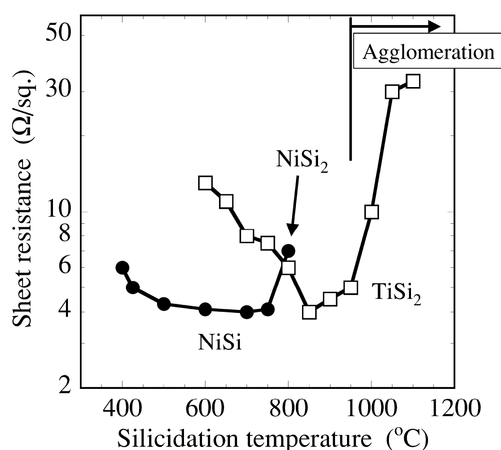


Fig. 43. Dependence of sheet resistance on the silicidation temperature.

3.3.2 Silicon consumption during the silicidation

Silicon consumption during the silicidation is a very important factor for salicide. Here, silicon consumption is defined as the distance between the initial silicon interface and the bottom of the silicide, as shown in Fig. 45. The distance is normalized by the silicide thickness and shown in Fig. 44. Because NiSi is monosilicide, the silicon consumption is basically smaller than that of disilicide. From Fig. 44, it is found that the NiSi silicon consumption is about 20% smaller than that of $CoSi_2$ case. This means that thickness of the silicide can be increased about 20% and the sheet resistance can be reduced by that amount. This is beneficial for ultra-shallow junctions for sub-100-nm node CMOS.

Silicide	Resistivity ($\mu\Omega$ cm)	Moving species	Silicidation temperature (°C)	Film stress (dyne/cm)	Si consumption
$TiSi_2$	10–15	Si	750–900	1.5×10^{10}	0.904
$CoSi_2$	18	Co	550–900	1.2×10^{10}	1.03
CoSi	>180	Si	400–600	–	–
Co_2Si	>180	Co	400	–	–
NiSi	20	Ni	350–750	6×10^{9}	0.82
PtSi	28–35	Pt	800	1×10^{10}	–
Pd_2Si	30–35	Pd, Si	800	1.3×10^{10}	–
WSi_2	70	Si	950	–	–
$MoSi_2$	100	Si	1000	–	–

Fig. 44 Summary of various salicide properties

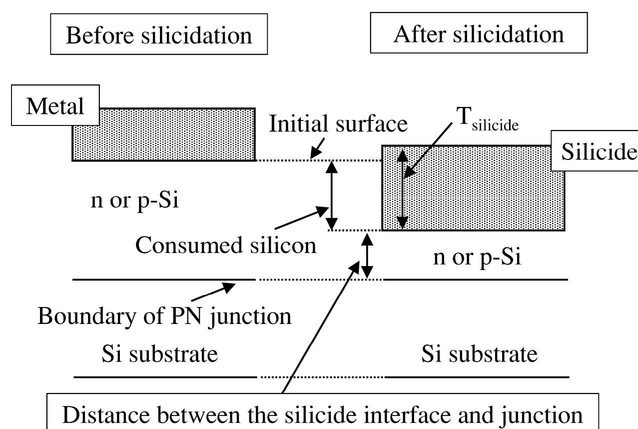


Fig. 45. Illustration explaining silicon consumption

3.3.3 Adverse narrow line effect

When the width of the $TiSi_2$ line becomes narrow, significant increase in the sheet resistance is observed, as shown in Fig. 46. This is called as 'narrow line effect'. There are two reasons for the increase. In the width range between 2.0 and 0.2 mm, the silicide is composed of the mixture of C54 (low resistivity) and C49 (high resistivity) crystals as shown in the TEM photograph in Fig. 47.

By the higher temperature of the second step anneal (for the $TiSi_2$ case), all the C49 films should transit to C54, but the transition becomes difficult when the width of the $TiSi_2$ line becomes small. In addition, when the width of the $TiSi_2$ becomes less than 0.2 mm, the grain of silicide is disconnected in the line by agglomeration phenomenon as shown in Fig. 48. The narrow line effects of TiSi2 can be suppressed by introducing additional process steps such as preamophization of the film by such as Mo or As shown in Fig. 46. While in the case of NiSi, the increase of the sheet resistance for the narrow line is not observed at all, because there is only NiSi crystal phase (low resistivity) in the wide process temperature range below 750℃. Even the sheet resistance of the narrow line becomes small in the NiSi case, as shown in Fig. 46. This is because the silicide film becomes thicker at the edge of the line, as shown in Fig. 49. In the case of Ni silicidation, Ni is the moving species for the reaction. The thicker silicide is formed at the edge since more Ni atoms are supplied there than the center to react with silicon as shown in Fig. 50. On the contrary, in the $TiSi_2$ case, Ti is the moving species and, thus, more Ti atoms diffuse into silicon at the edge, resulting in thinner films at the edge. In the case of Cobalt silicide, there are many phase, Co_2 Si (high resistivity), CoSi (high resistivity)

and $CoSi_2$ (low resistivity), and the situation is complicated, but the adverse narrow line effect was usually not observed. Similar phenomenon of thickness increase at the edge of line as NiSi was observed.

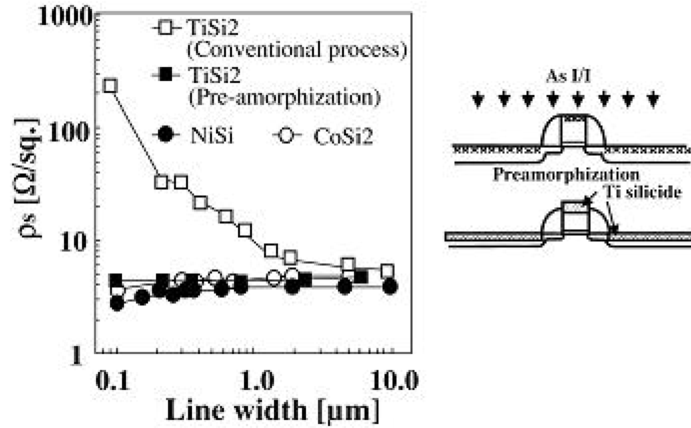


Fig.46. Dependence of sheet resistance on line width for various silicide materials.

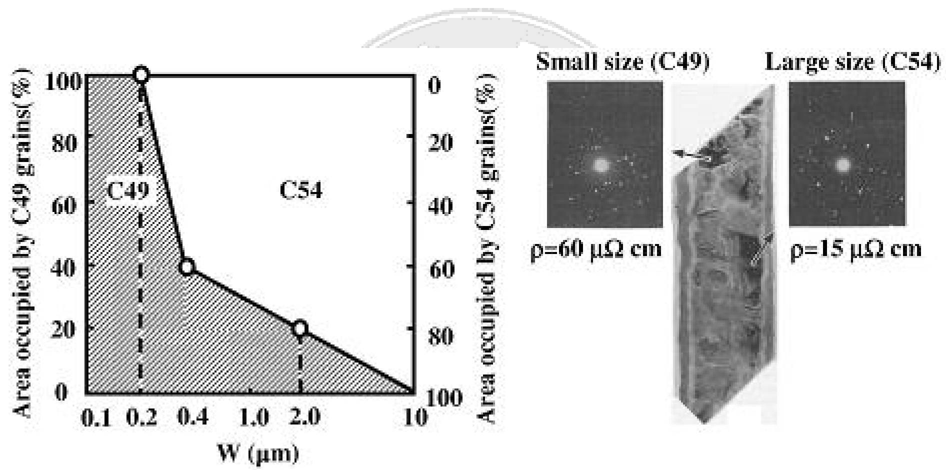


Fig. 47. Relationship between crystal structure and TiSi2 line width.

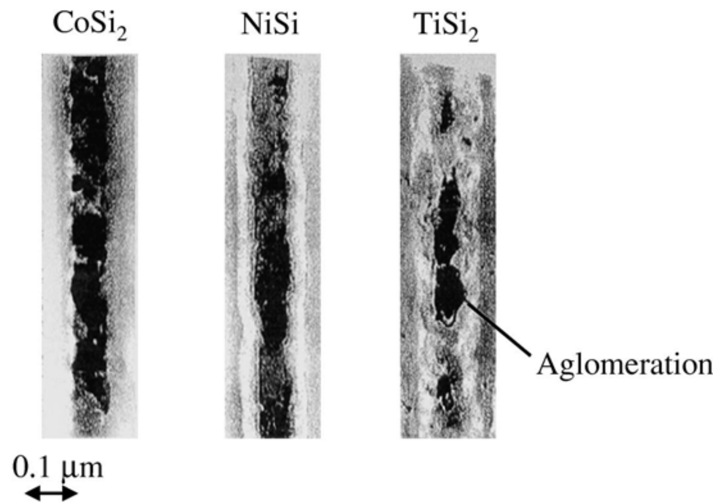


Fig. 48 TEM images of 0.1 mm TiSi , NiSi, and CoSi lines.

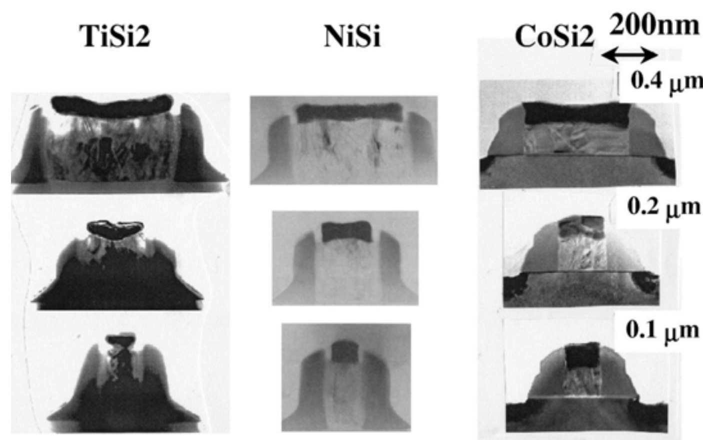


Fig.49. TEM images of cross-section of TiSi , NiSi, and CoSi lines

(a) Si diffusion case ($TiSi_2$). (b) Metal diffusion case (NiSi, $CoSi_2$).

Fig.50. Schematic cross-section of moving species during silicidation at the edge of the poly Si gate electrode.

3.3.4 Bridging failure

Silicide formation on the gate sidewall can result in short-circuit failures between the gate and source / drain terminals. Such failure sometimes occurs in the case of $TiSi_2$, because moving species of the silicidation is Si as shown in Fig. 44, and sometimes Si atoms diffuse into the Ti film on the sidewall portion and form a silicide salicide, as shown in Fig. 51a. On the other hand, Ni silicidation proceeds by the diffusion of Ni into silicon area as shown in the table, and thus, there is no possibility for the silicide later formed at the sidewall as shown in Fig. 51b. This is a great advantage of NiSi salicide. For the case of $TiSi_2$ silicide, the bridging failure is suppressed by two-step silicidation. In the first step, the Ti film deposited on MOSFETs was silicided at low temperature such as 600℃. In the low temperature, silicidation reaction was not very strong and the possibility of the aggressive diffusion of Si into the sidewall portion of the Ti metal is small. Then, non-silicided Ti film on the sidewall is etched off by acid solution. C49 TiSi is, then, converted to the C54 TiSi by the second anneal

at 800℃. In the case of $CoSi_2$, the possibility of the bridging can be avoided also by the second step silicidation. In this case, Co film is converted to Co_2 Si in low temperature anneal, such as at 450℃. In the case of Co_2 Si formation, Co atom is the moving species and there is no possibility of the bridging. Then, after the removal of the non-reacted Co film, Co Si is converted to CoSi via CoSi phase at high temperature, such as at 750℃. In the case of one-step anneal, bridging of $CoSi_2$ was observed, but it was confirmed that the bridging is completely suppressed by the two-step silicidation. In the case of $TiSi_2$, however, the bridging possibility cannot be completely neglected because of the silicidation mechanism — or moving species. In the case of NiSi, there has been no bridging failure at all because of the silicidation mechanism.

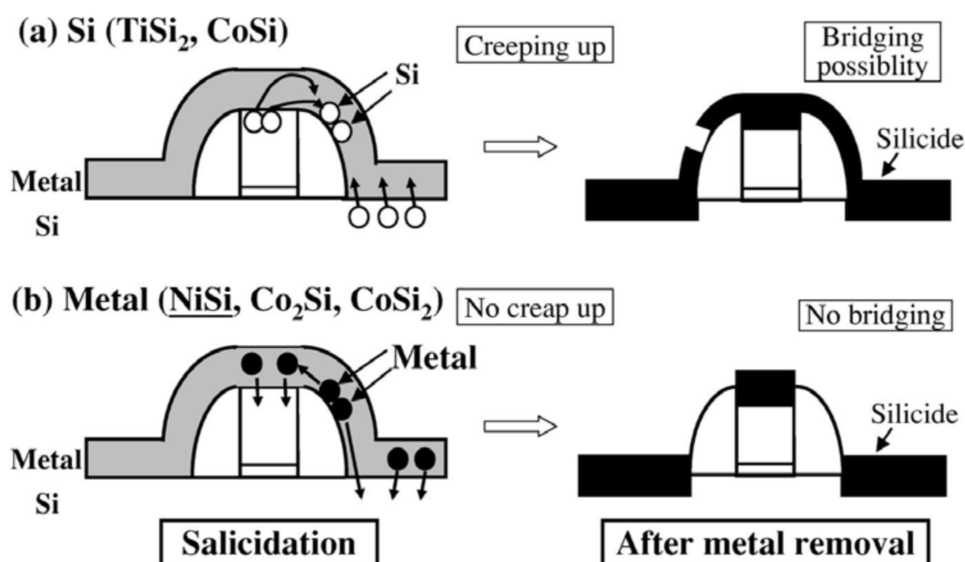


Fig.51 Schematic cross-section of moving species during silicidation at the gate sidewall.

3.4 Experimental

Ni/poly-Si/dielectric stacks were deposited on (100) Si wafers, for varying film thickness, in the 30-170 nm and 60-100 nm ranges for Ni and Si films, respectively. Dielectric films used in this study included SiO2, SiON, HfSiON and HfSiON/SiO2 stacks of varying thickness with equivalent oxide thickness (EOT) in the 1–20 nm range. Samples were reacted by rapid thermal processing (RTP) to form silicide films at temperatures in the 280–850℃ range, typically for 30–60s. A wet etch used in self-aligned Ni silicide processes (diluted sulfuric-peroxide solution) was subsequently performed. In some samples a second RTP anneal step was performed after the selective

etch. Samples were characterized by X-ray diffraction (XRD) using Cu Kα radiation and scanning electron microscopy (SEM). Patterned FUSI gate devices were also fabricated for electrical characterization, using a chemical-mechanical polishing (CMP) flow previously described or a conventional flow (the latter used only for fabrication of capacitors overlapping isolation). A CMP flow with a patterned poly-Si etch back step was used for fabrication of phase controlled dual WF Ni FUSI CMOS circuits.

3.5 Results and discussion

3.5.1 Ni silicide phase formation and effective work function

Fig. 52 shows a schematic of the Ni-Si reaction path. After formation of Ni-rich silicides, two branches are possible in the reaction path, depending on whether Ni or Si is consumed first. NiSi2 nucleates at higher temperatures (if Si is still available). For Ni to Si atomic ratios between 1 and 2, Ni3Si2 can grow by reaction of NiSi with the Ni-rich silicides. On the other hand, if Si is fully consumed after initial growth of the Ni-rich silicides, NiSi cannot nucleate. Ni31Si12 and Ni3Si are observed in this case with increasing thermal budget, provided sufficient Ni is available. Fig. 53 shows the XRD spectra of FUSI samples for the different silicide phases, obtained by controlling the deposited Ni to Si thickness ratios and using sufficient thermal budgets to drive the reactions to completion. The effective WF of several Ni silicide phases on HfSiON and SiO_2 are shown in Fig. 54. A significantly higher WF is seen for the Ni-rich silicides compared to NiSi on HfSiON.

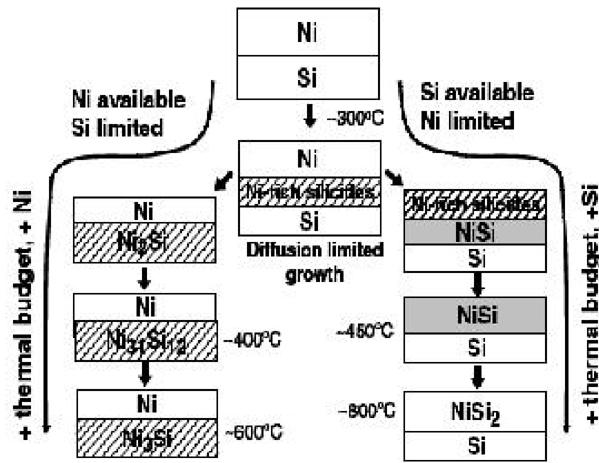


Fig. 52 Schematic of Ni–Si reaction path.

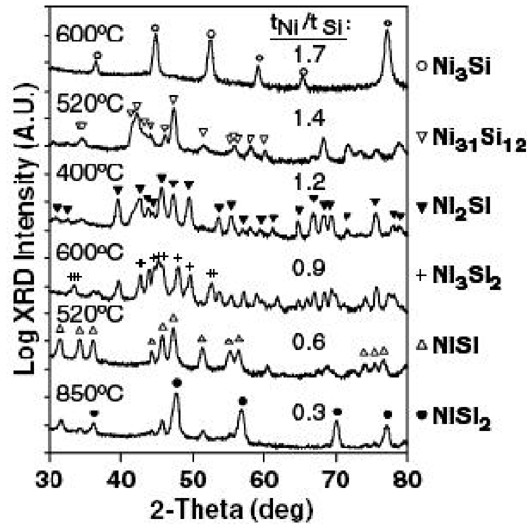


Fig. 53 X-ray diffraction patterns (Cu Kα radiation) showing formation of the different Ni silicide phases controlled by the Ni to Si thickness ratio (tNi/tSi). Temperatures of RTP reaction are indicated.

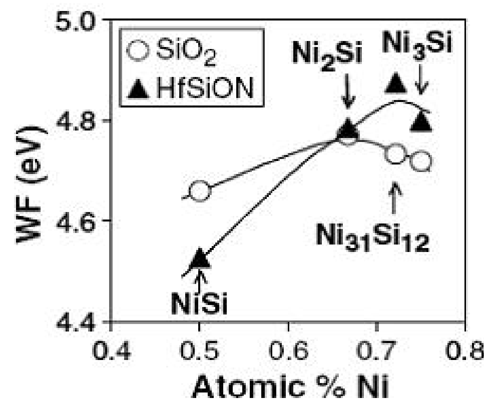


Fig. 54 Effective work functions of several Ni silicides on HfSiON and on SiO2 dielectrics.

3.5.2 Scalability of Ni FUSI gate processes and device implementation

On small patterned structures, control of the silicide phase is not easily achieved by simply controlling the deposited Ni to Si thickness ratio. Ni available from areas surrounding small devices can diffuse and react with poly-Si in the gate to increase the effective (reacted) Ni to Si ratio (Fig. 55). When targeting NiSi, for example, a deposited Ni to Si thickness ratio of 0.6 results for large structures in a stack with a NiSi layer in contact with the dielectric interface and a layer of Ni-rich silicide on top, when the thermal budget of the reaction is high enough to form NiSi. In Fig. 56, the sheet resistance as a function of linewidth is plotted for the reaction of 60 nm Ni with 100 nm poly Si at 520 ℃ (30s). The low sheet resistance for wide lines corresponds to the presence of NiSi. For narrow lines, however, an increase in sheet resistance is observed, which can be attributed to the formation of a thicker Ni-rich silicide (and little or no NiSi). In Fig. 56 it can be seen that there is good agreement between the sheet resistance at narrow linewidths obtained for 60 nm Ni using the 1-step RTP process (520℃) and the sheet resistance of a Ni-rich silicide obtained from 170 nm Ni. In order to control the silicide phase of FUSI gates at arrow linewidths, a 2-step RTP process is used (Fig. 56). The reacted Ni to Si ratio is controlled in this process by the thermal budget of the first RTP step (RTP1). After selective Ni etch, no additional Ni is available for the reaction during the RTP2 step (used to form NiSi) and the Ni to Si ratio remains unchanged. Fig. 57 illustrates the RTP1 process window for a 2-step RTP process targeting NiSi FUSI gates (NiSi at interface with the dielectric) and using 100nm poly-Si. Calculated using measured Ni silicidation kinetic data, for a reaction not limited by Ni availability (which can be the case at short gate lengths). At low RTP1 thermal bud- gets, insufficient Ni is reacted and the gates remain incompletely silicided after the RTP2 step. At high thermal budgets, a Ni-rich FUSI gate is formed. The process window for NiSi FUSI gates is seen to be narrow. Further more, since the morphology of the films cannot be expected to be ideal (layered structure with planar interfaces) and in order to account for process variability, additional margins need to be added, reducing the effective process window. Fig. 58 shows the Vt roll-off of Ni FUSI / HfSiON devices for several processes. This corresponds to the transition form NiSi FUSI gates at long gate lengths to Ni-rich FUSI gates at short gate lengths, in agreement with the corresponding WF values (see Fig. 54). This step is

eliminated with the optimized 2-step RTP process, obtaining a smooth Vt roll-off curve indicating that the NiSi phase in contact with the dielectric is maintained at all gate lengths. Finally, a process targeting Ni-rich silicided gates is shown as well, achieving a smooth Vt roll-off. From these plots, and considering the requirement of low Vt values for scaled CMOS technologies, it is clear that NiSi is more attractive for NMOS devices on HfSiON, while Ni-rich silicides are more attractive for PMOS applications.

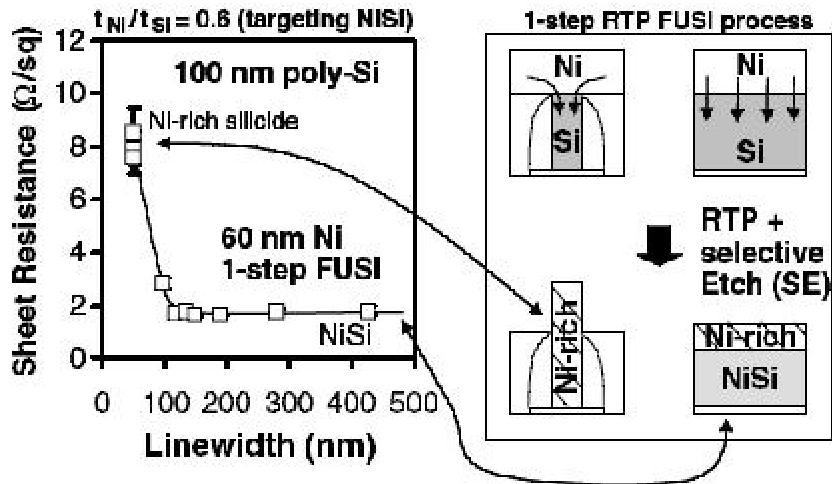


Fig. 55 The sheet resistance for a 1-step RTP FUSI process targeting NiSi increases on narrow gates (left). This is attributed to full silicidation of the narrow gates with a Ni-rich silicide, due to the diffusion of Ni from surrounding areas resulting in a higher effective Ni–Si ratio (right).

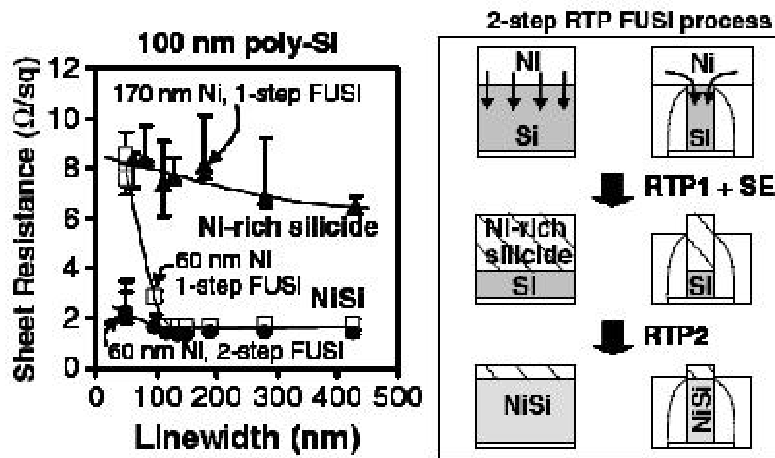


Fig. 56 Sheet resistance vs. linewidth for Ni FUSI gates fabricated by reaction of a Ni film with 100 nm poly-Si (left). A Ni-rich silicide is obtained for 170 nm Ni using a 1-step RTP process. A linewidth effect is observed for 60 nm Ni using a 1-step process. This is eliminated by using an optimized 2-step RTP process which results in a NiSi FUSI gate (right).

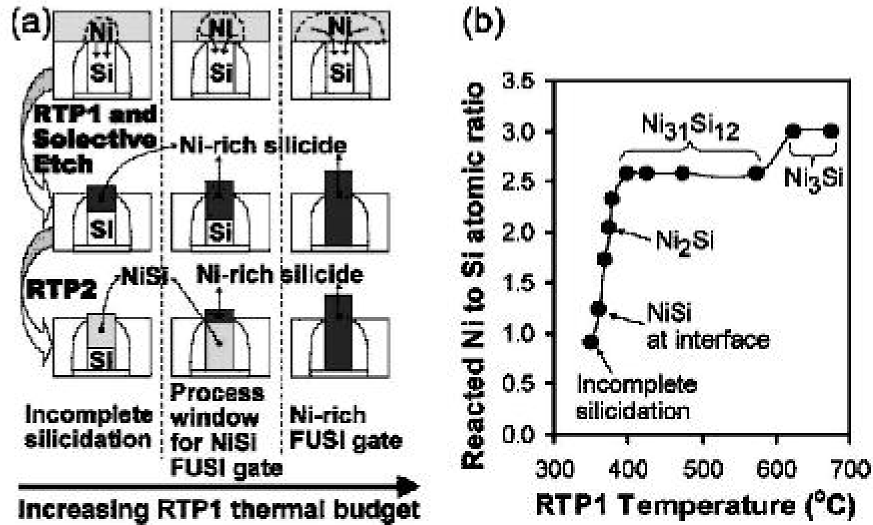


Fig.57 (a) Schematic of the two-step RTP silicidation process. At short gate lengths, the reacted Ni-to-Si ratio increases with increasing RTP1 thermal budget due to Ni diffusion from areas surrounding the gate. The reacted Ni- to-Si ratio and resulting silicidephase can be controlled by the RTP1 thermal budget. The RTP2 step is used to drive the reaction to completion. (b)Reacted Ni-to-Si ratios extracted from RBS analysis as a function of RTP1 temperature for 100 nm poly-Si.

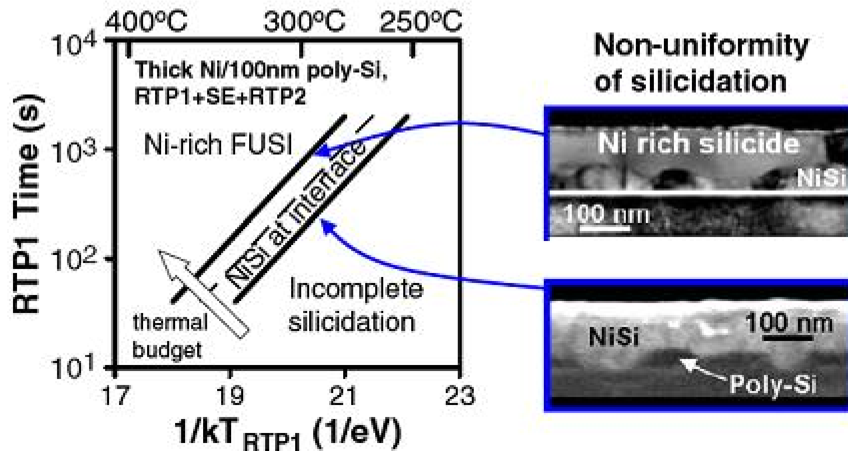


Fig. 58 RTP1 process window for a 2-step RTP process targeting NiSi gates (NiSi at interface with dielectric), calculated based on Ni silicidation kinetics. A Ni2Si/NiSi stack is assumed within the process window (solid lines), presence of Ni3Si2 would further reduce the process window (upper limit of RTP1 thermal budget, assuming a Ni3Si2/NiSi stack, shown in dashed lines). Margins should be added to account for interface roughness and non-uniformity of silicidation.

3.5.3 Dual work function phase controlled Ni FUSI CMOS integration scheme

For bulk Si CMOS technologies, in order to achieve tar- get Vt values, it is desirable to use a high effective WF (4.8-5.2 eV) material on PMOS devices and a low WF material (4.0-4.4 eV) on NMOS devices. As discussed in the previous section, the change in effective WF with Ni silicide phase on HfSiON opens an interesting opportunity for dual WF metal gate CMOS integration. Fig. 49 shows the integration scheme we propose to use, to achieve NiSi FUSI gates on NMOS devices and Ni-rich FUSI gates on PMOS devices. Following the CMP flow for fabrication of FUSI devices previously described, and before the FUSI module, a patterned poly-Si etch back step is used to reduce the poly-Si height on the PMOS devices. An optimized 2-step RTP FUSI process is then used to silicide simultaneously NMOS and PMOS gates. This approach was demonstrated, including the fabrication of working ring oscillators. Fig. 60 shows cross-sections of NMOS (NiSi FUSI gate) and PMOS (Ni-rich FUSI gate) transistors fabricated on the same wafer using this flow. Device characteristics obtained are shown in Figs. 61 (Vt roll-off).

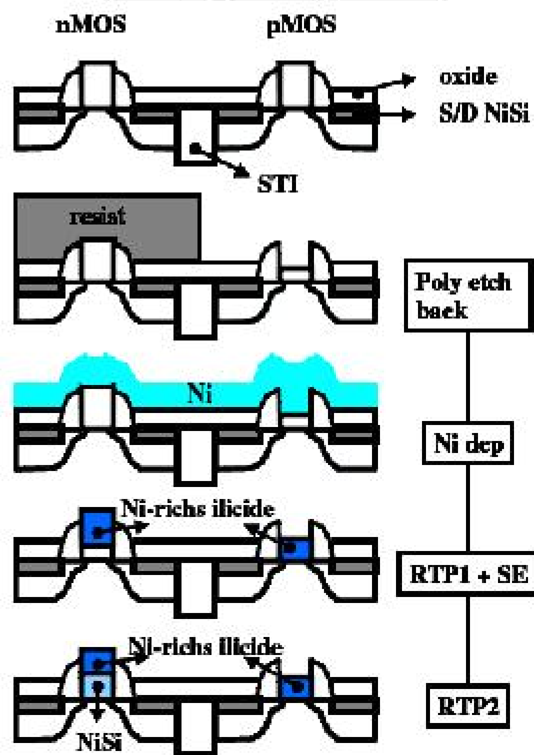


Fig. 59 Schematic of dual WF phase controlled Ni FUSI CMOS integration scheme using poly-Si etch-back on PMOS.

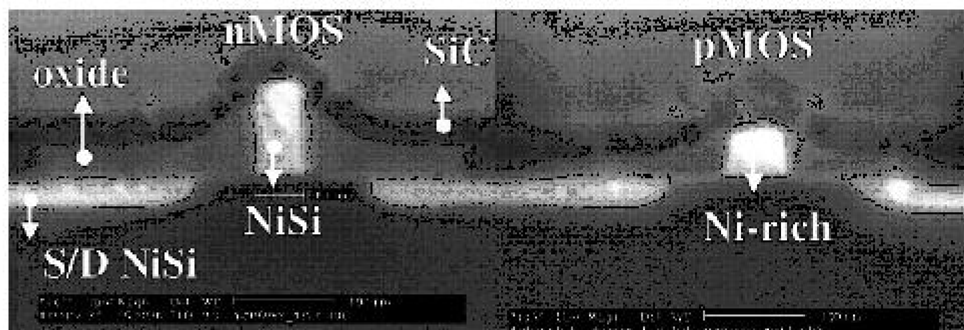


Fig. 60 SEM cross-sections of NMOS NiSi FUSI gate (left) and PMOS Ni-rich FUSI gate (right) devices fabricated on the same wafer using the dual WF CMOS integration scheme shown in Fig. 59

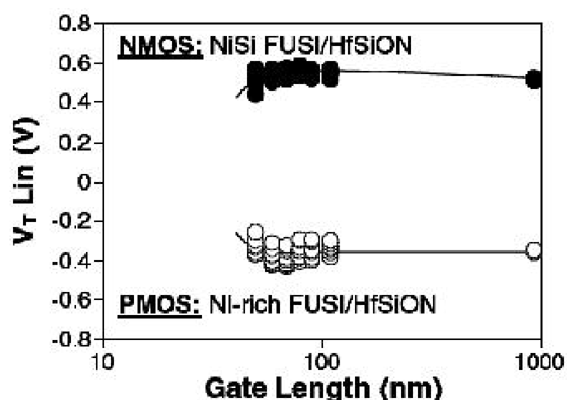


Fig. 61 Linear Vt roll-off for devices built using the CMOS dual WF phase controlled FUSI flow shown in Fig. 59.

3.6 Conclusions

The scalability issues of Ni FUSI gates were discussed, showing phase control at short gate lengths to be a key concern. A linewidth effect was found for processes targeting NiSi FUSI gates with non-optimal thermal reaction, which resulted in formation of Ni-rich FUSI gates at short gate lengths. An optimized 2-step RTP process was shown to solve this issue achieving good scalability for NiSi FUSI gates. Scalable processes for Ni-rich FUSI gates were also demonstrated. A dual WF Ni FUSI / HfSiON CMOS integration scheme, using a poly-Si etch back step and simultaneous silicidation of NMOS and PMOS was demonstrated and used to fabricate circuits with NiSi FUSI gates on NMOS devices and Ni-rich FUSI gates on PMOS devices.

Chapter 4 Electroless Plating

4.1 Introduction

Along with semiconductor industry in during several years rapid development, process technology unceasingly progresses for CMOS devices to keep up with the downscaling and into ULSI nodes. The metallization process has become an extremely important essential step. In the semiconductor technology node, the metal thin film function mainly is Ohmic Contact, Schottky Barrier Contact, Gate electrode and interconnects. However, silicide in the semiconductor circuits function mainly is Ohmic Contact or Interconnect for reduce contact resistivity to improved RC delay.

This research in choice of material, because silicide of nickel has low resistance and few silicon consumption, the NiSi is the main material. On the other hand, for the semiconductor manufacture process, deposition of NiSi by chemical displacement and electroless plating onto a silicon layer can form ultra-shallow junction different to CVD (Chemical vapor deposition) and ITM (implant through metal) are obtained simultaneously, therefore improve short-channel effects (SCEs), achieves the device downscaling goal.

For a CMOS technology to keep up with the downscaling, in order to reduce short-channel effects (SCEs) and RC delay. Fig. 62 is show structure of MOSFET. Fig. 63 is show materials effect of MOSFET downscaling. To understand the shallow junction and low parasitic source / drain (S / D) resistance are required. Self-aligned silicide is wildly used in CMOS process manufacturing to reduce sheet resistance of source and drain.

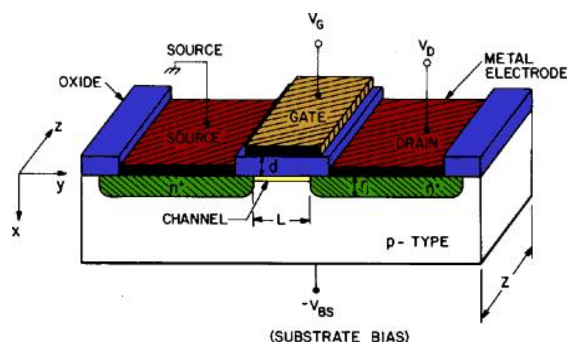


Fig. 62 Structure of MOSFET

【Selective Deposition NiP as Diffusion Source to Form n+p Junction and NiSi Simultaneously】

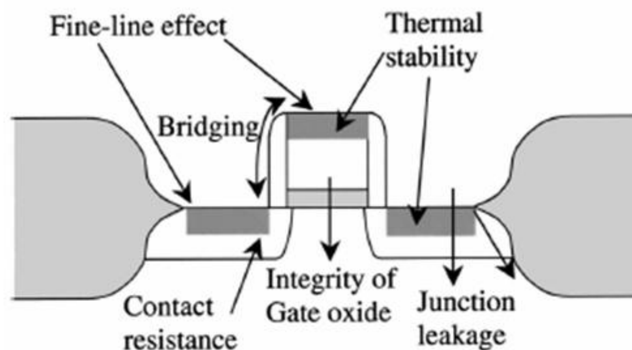


Fig. 63 Materials effect of MOSFET downscaling

【Selective Deposition NiP as Diffusion Source to Form n+p Junction and NiSi Simultaneously】

Al was used reduce resistance of gate and metal junction. Because of in integrated circuit temperature regular meeting to achieve 450-500℃, reaches as high as 0.5-1at.% in this temperature range silicon in the Al solubility, and in the aluminum thin film the rapid proliferation causes in the contact surface production hole. This was called aluminum spiking question. Fig. 64 is show Si dissolution in the aluminum. Aluminum spikes could punctuate through the doped junction, short source / drain with the substrate, and damage the devices. Fig. 65 is shows spike effect. Because of Al spike effect and process temperature limit. Therefore from 1966, he metal silicide technology is applied reduces to the Ohmic contact and the Schottky contact resistance. In 1979, the high conductive metal silicide is used to form polyside structure with the poly silicon. In 1981, Self-aligned silicide (salicide) technology was extends form silicon the contact window to the gate polycide and source/drain diffusion area. Fig. 66 is show generalization structure of salicide and Fig. 67 is shows manufacture step of salicide.

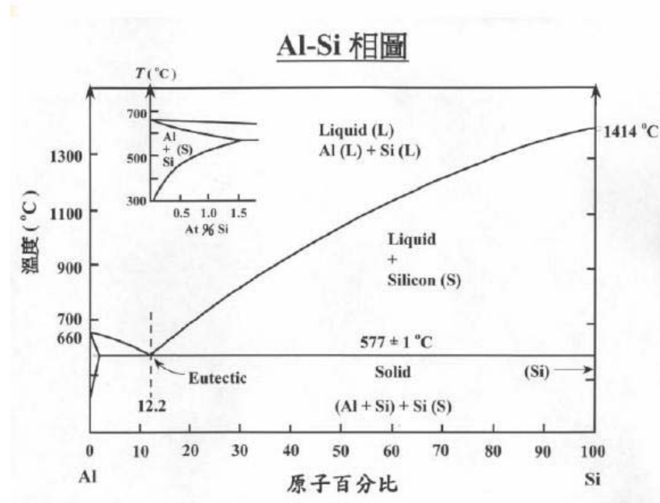


Fig. 64 Al and Si Eutectic reactions

【Introduction to Semiconductor Manufacturing Technology】

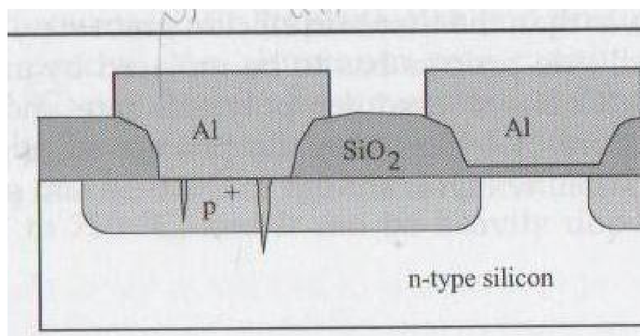


Fig. 65 Spike effect of Al-Si

【Hong Xiao,"Introduction to Semiconductor Manufacturing Technology】

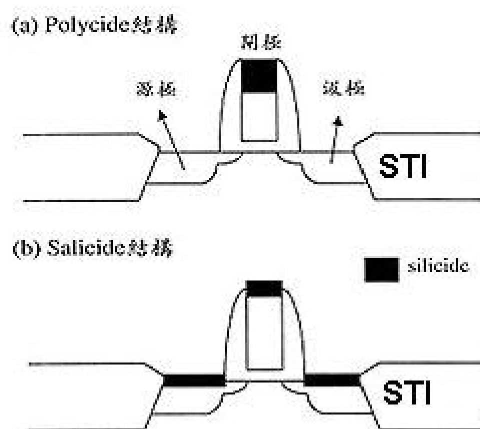


Fig. 66 (a) Polycide and (b) Salicide gate structure

【林鴻志,"深次微米閘極技術之發展與未來驅勢(II)】

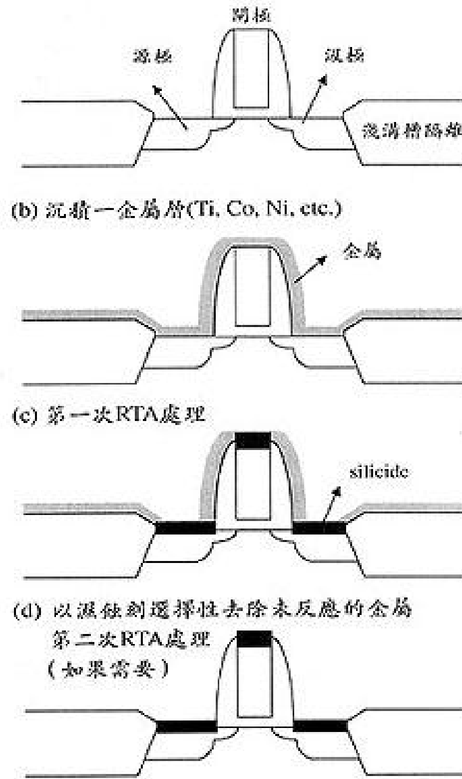


Fig. 67 Manufacture step of salicide

【林鴻志,"深次微米閘極技術之發展與未來驅勢(II)】

Ti, Co and Ni are used for the preparation of metal silicide process. Titanium silicide has some disadvantages in the downscaling of MOSFET such as Bridge Short Effect and narrow linewidth effect. Fig. 68 is show Bridge Short Effect of silicide. Titanium silicide nucleus decrease when linewidth downscale is causing not change the Titanium C49 from to the Titanium C54, so Titanium silicide resistivity in increase as linewidth decrease. The effect was called the narrow linewidth effect. Fig. 69 is show narrow linewidth effect of Titanium silicide. Formation of cobalt silicide has some disadvantages such as very high Si consumption and agglomeration. Low resistivity NiSi has attracted great attention as contact to source/drain and gate of CMOS and formation of Nickel silicide has little Si atom consumption. Fig. 74 is shows Compare of TiSi2, CoSi2, NiSi.

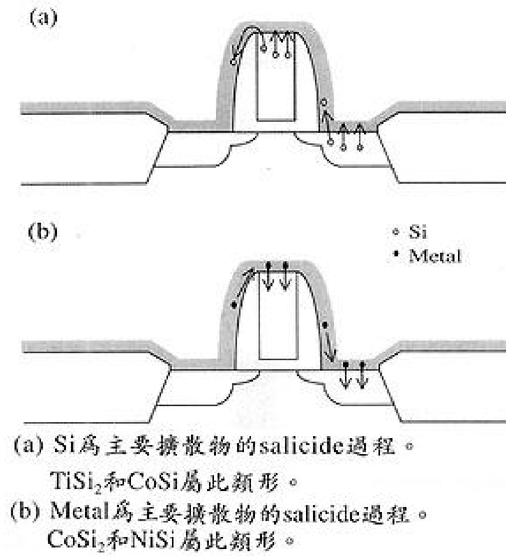


Fig. 68 Bridge short effect of silicide.

【林鴻志,"深次微米閘極技術之發展與未來驅勢(II)】

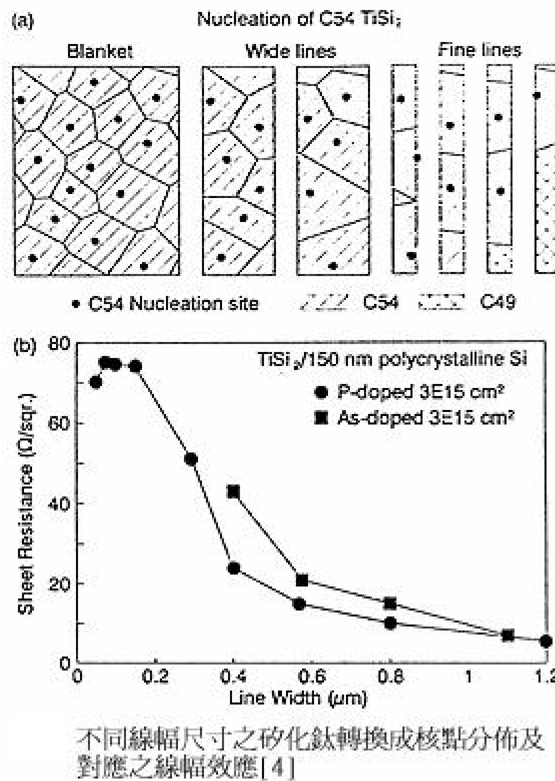


Fig. 69 Narrow linewidth effect of Ti silicde

【林鴻志,"深次微米閘極技術之發展與未來驅勢(II)】

Salicide	$TiSi_2$	$CoSi_2$	NiSi
Resistivity (uOhm-cm)	13-20	14-20	14-20
Formation Temperature (° C)	600-700	600-700	400-600
Melting Point (° C)	1500	1326	992
Eutectic Point (° C)	1330	1204	964
Thermal Stable Point (° C)	<950	900	700
Schottky Barrier Height (eV)	0.6	0.64	0.67
Selective etch solution	$NH_4OH:H_2O_2$	$HCl:H_2O_2$	$HNO_3:HCl$
Major migrate atom	Si	Co	Ni
Consume Silicon Ratio	2.27	3.64	1.83
Formed Salicide Ratio	2.51	3.52	2.34

Fig. 74 Comparison table of metal salicide materials

【 Meng-Chi Chen, Chen*, Yean-Kuen Fang**,, "The Studies of Contact Reactions Among Tungsten Plug, Copper Plug, CoSi2 and NiSi in Deep Submicron ULSI Technology ", Department of Electrical Engineering National Cheng Kung University】

In 1846, A. Wurtz has found precipitate of reducing Nickel metal in the nickel hypophophite solution when heats up 100℃. In 1911, P. Breteau to analyse the nickel hypophophite solution behavior, explains this response for own self-catalytic reaction and the resultant has the composing of phosphorus. In between 1946 and 1947, A. Brenner and G. Riddell service in the American National Standards Institute (ANSI) was found a strong reduction of sodium hypophosphite by investigate plating nickel on the steel. A. Brenner and G. Riddell is inventor of electroless plating. Therefore, deposition of NiSi by chemical displacement and electroless plating onto a silicon layer can operation easily, low cost and co-deposition phosphorus different to ITM (implant through metal).

4.2 Experimental

4.2.1 Chemical deposition of Ni on Si and SiO_2

Taking sample were 2 × 3 cm on the p-type wafer. They were cleaned by RCA clean process method. After cleaning, the sample was immersed in HF solution pretreatment remove native oxide. After remove native oxide, the sample was immersed in 0.5M $(NH_4)_2SO_4$ and 0.05M ethanol mixed solution for 5 minutes. Deposition of Ni on SiO_2 was used the same process, but not

immersion the HF solution. Si and SiO_2 sample was dipped in Ni bath of Fig. 75. Surfaces of Si and SiO_2 were examined by FE-SEM. Fig. 75 is show composition and operation of bath.

	Ni Bath	NiP Bath
$NiSO_4 \cdot 6H_2O$	0.1 M	0.1 M
$(NH_4)_2SO_4$	0.5 M	0.5 M
$NaH_2PO_2 \cdot H_2O$	—	0.1 M
NH_4OH	1M	1M
Ethanol	0.05 M	0.05 M
pH	9	9
Temperature	70 ℃	60℃
Time	5 min	75 sec

* All solutions were purged by Ar to remove the dissolved oxygen

M（莫耳濃度）：mol/L

Fig. 75 Composition and operation of bath

【Selective Deposition NiP as Diffusion Source to Form n+p Junction and NiSi Simultaneously】

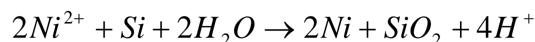
4.2.2 Chemical co-deposition of Ni and P on Si

Immersing the Si sample in NiP bath of Table 2. The Si sample form NiSi and doping phosphorus on the Si by RTA process. Microstructures of sample were analyzed by FE-SEM, GID and SIMS.

4.3 Results and Discussions

4.3.1 Selective of displacement

The deposition of Nickel on Si layer is induced by following Redox reaction:



$$2Ni^{2+} + Si + 2H_2O \rightarrow 2Ni + SiO_2 + 4H^+$$

The equilibrium potential for this reaction can be represented by the Nernst equation:

$$E = E^0 - \frac{2.3RT}{4F}\ln\left(\frac{Si^{4+}}{(Ni^{2+})^2}\right)$$

The E value is decreasing with decreasing Ni^{2+} concentration. Because of we use NH_4OH as complexing agent to form Ni ammine complex ion, therefore reaction in the low temperate will be obtained. Fig. 70(a) is shows using EDX to analyze Ni deposition on Silicon layer. Fig. 70(b) is show using EDX to analyze Ni deposition on SiO_2 layer. The Fig. 70 is explains the Ni displacement deposition on Si , but it is not displacement on SiO_2 surface.

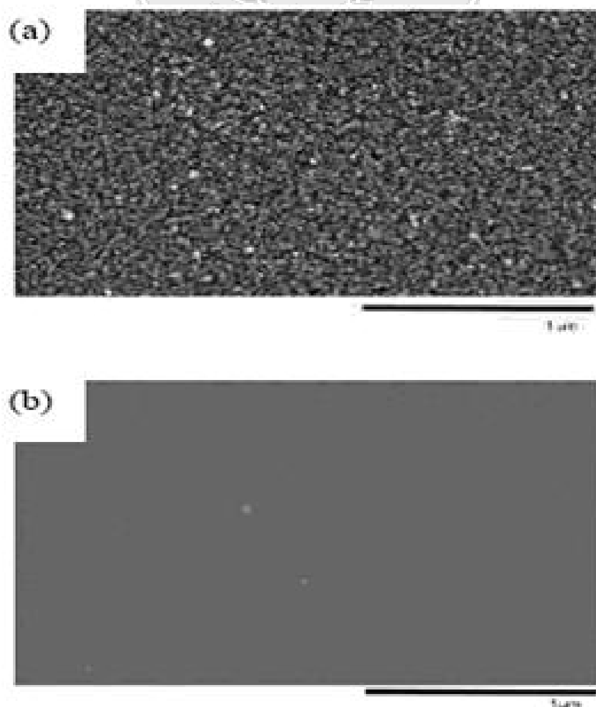


Fig. 70 Micrographs of Ni deposits on (a) P-type Si substrate (b) SiO2 substrate

【Selective Deposition NiP as Diffusion Source to Form n+p Junction and NiSi Simultaneously】

4.3.2 Formation of junction and NiSi layer

Addition of sodium hypophosphite in NiP bath of Fig. 75 is effective for the co-deposition of Ni and P. After deposition of Ni-P by RTA process, phosphorous drive in into NiSi layer can application to form N^{+}/P ultra-shallow junction on Si layer. Fig. 71 is showed using FE-SEM to analyze NiSi thickness on Silicon layer increase at different RTA temperatures. The Fig10 is explains to change the Ni-P from the NiSi on the Si surface by RTA process. Fig. 72 is show using GIXRD to analyze composition of silicon surface at different RTA temperatures. The Fig. 72 is explains to change the Ni_3P from the NiSi when RTA temperatures up to 550℃. Fig. 73 is show using SIMS to analyze element profile of depth. The Fig. 73 is explains phosphorous drive in NiSi layer on the Si surface.

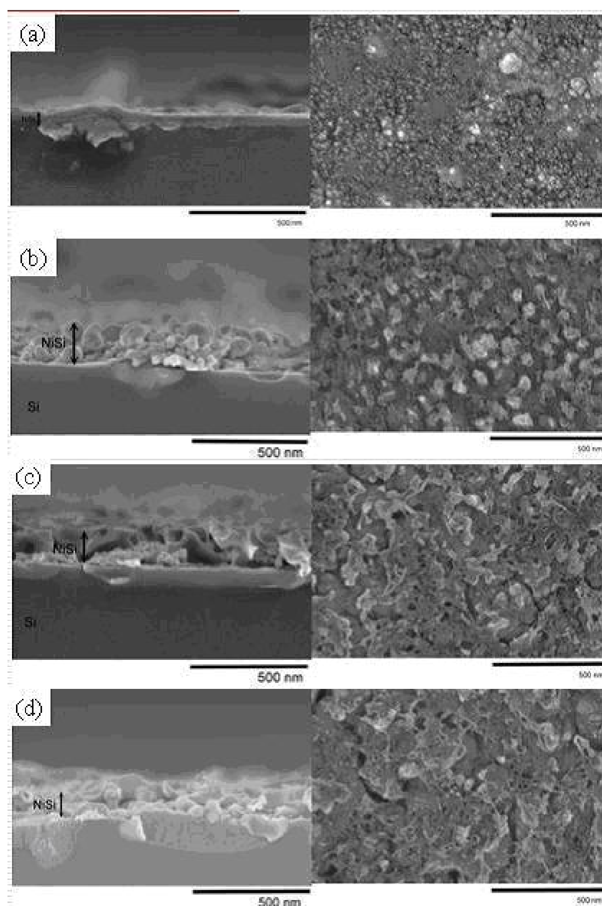


Fig. 71 (a) 500oC, thickness: 50nm
(b) 550oC, thickness: 160nm
(c) 600oC, thickness: 175nm
(d) 650oC, thickness: 185nm

【Selective Deposition NiP as Diffusion Source to Form n+p Junction and NiSi Simultaneously】

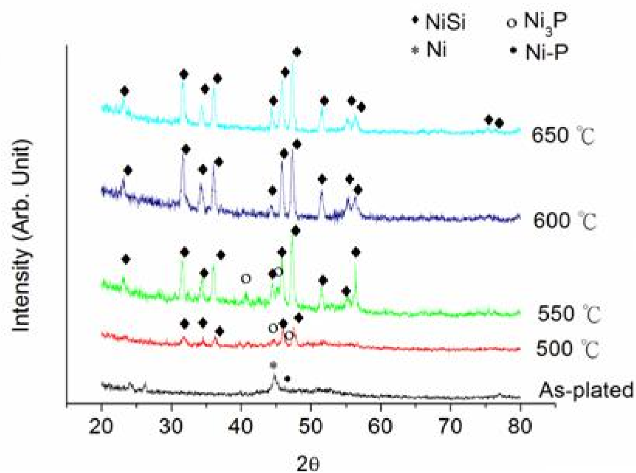


Fig. 72 Composition of silicon surface

【Selective Deposition NiP as Diffusion Source to Form n+p Junction and NiSi Simultaneously】

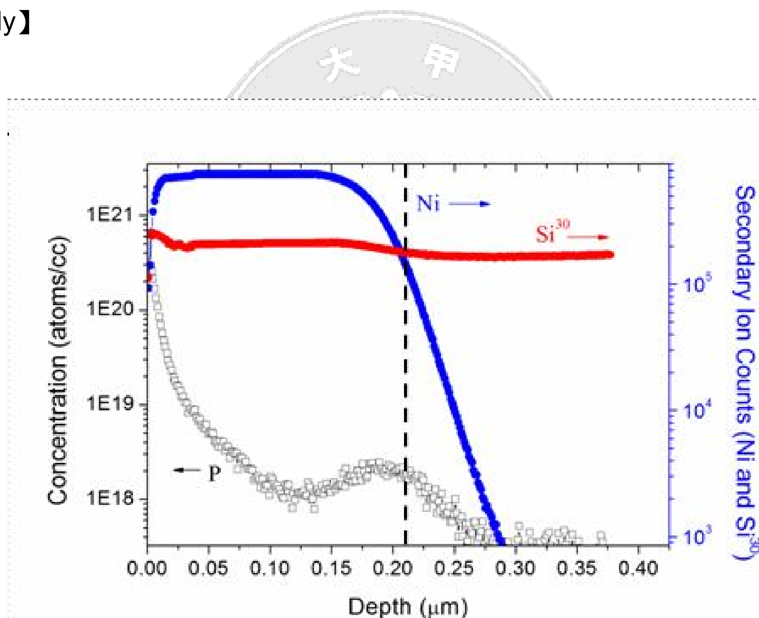


Fig. 73 Element profile of depth

【Selective Deposition NiP as Diffusion Source to Form n+p Junction and NiSi Simultaneously】

4.4 Conclusions

Electroless Nickel on Silicon layer is provides one kind of new ponder direction for Front-end of line (FEOL) of semiconductor processing. Nickel is not deposition on the SiO_2 layer, it has not the chemical displacement of nickel. Addition of NaH_2PO_2 to nickel ion bath will cause Ni and P co-deposition via chemical displacement and electroless plating. After RTA annealing above 550 ℃ , n+/p Ultra-Shallow Junction and NiSi diffusion layer are obtained simultaneously.

Chapter 5 Flash

5.1 Abstract

Non-Volatile Memory (NVM) has been developed and improved in past years, and recently it has been received much attention in mobile or portable applications, such as mobile phones, smart cards and digital camera. In last decade, Non-Volatile Memory (NVM) has been becoming more and more important in the semiconductor industry development. In the volatile memory market, DRAM is and will be the major choice of memory. However, the flash memory segment is growing faster than DRAM and SRAM recently. Since 2000, the flash memory market was growing lager than that of SRAM. It can be attributed to two major reasons. One is that many applications utilized NVMs for code storage. The other one is that NVMs have been applied in portable and mobile applications for data storage.

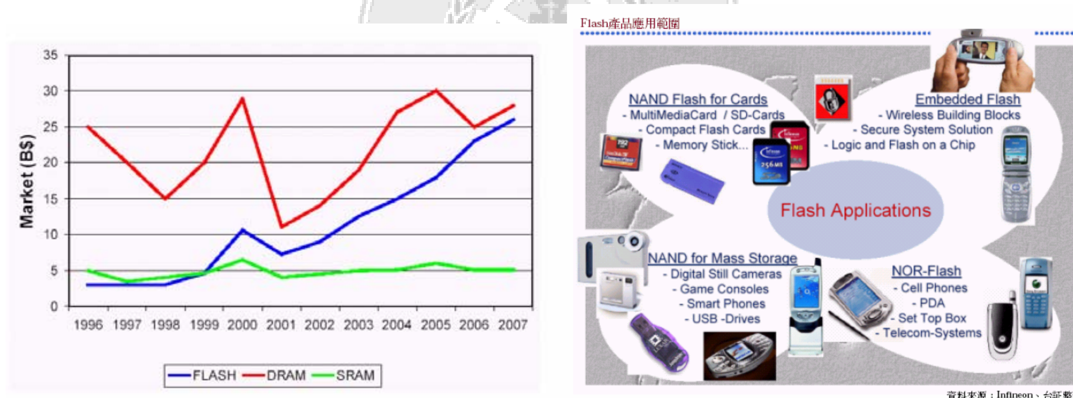


Fig. 76 Flash develop trend and applications

【工研院奈米電子元件技術組 高明哲(非揮發性記憶體)】

5.2 History

Since the metal-nitride-oxide-silicon(MNOS) was first explored in 1967 by Wegener et al.,NVMs have been manufactured over thirty years. First, the history of the Non-Volatile Memory (NVM) and the concept of the NVM are introduced. And the typical NVMs, such as EPROM(Erasable Programmable Read-Only-Memory), EEPROM (Electrically Erasable Programmable Read-Only-Memory), and flash memory are also introduced. Nowadays,

Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) becomes the most popular charge-trapping device because of its complete compatibility with existing advanced CMOS technology.

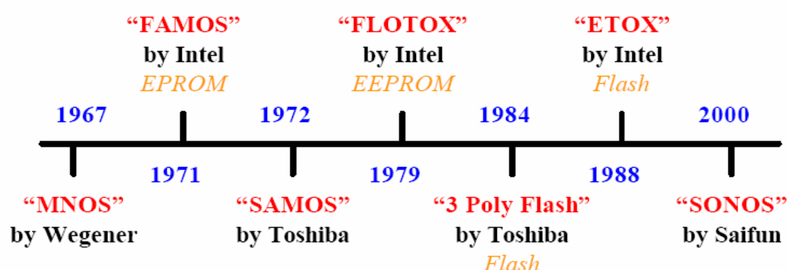


Fig. 77 The history of Nonvolatile Memory (NVM)

【中原大學：The Study of Si-implanted Oxide-Nitride-Oxide(ONO) for Memory Applications(郭百均).】

5.3 NOR and NAND

Many types of cell array architectures of flash memories have been proposed and developed. The two kinds of cell-array-architectures are so called NOR and NAND types. The schematic diagrams of the NAND and the NOR architecture. The NOR architecture of Flash memories which is usually used for ode Storage are manufactured by four major corporations: Intel、AMD、Fujitsu and Sharp; The NAND architectures of Flash memories which is usually used for ata Storage are manufactured by three other major corporations：Toshiba、Samsung、SanDisk.

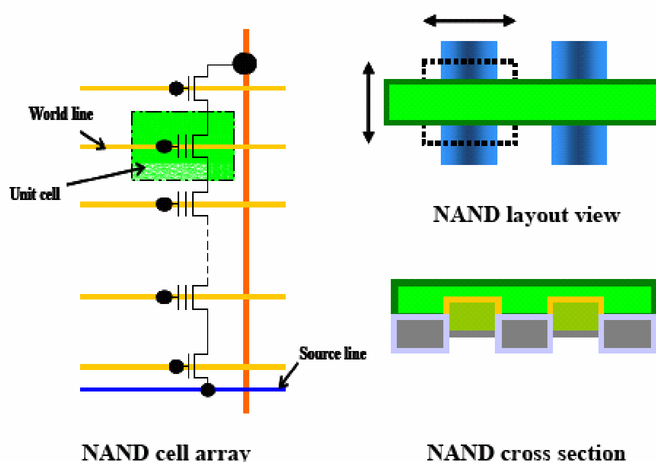


Fig. 78 The schematic cell array、layout view and cross section of the NAND architecture.

【中原大學：The Study of the novel NVM device(洪志學)】

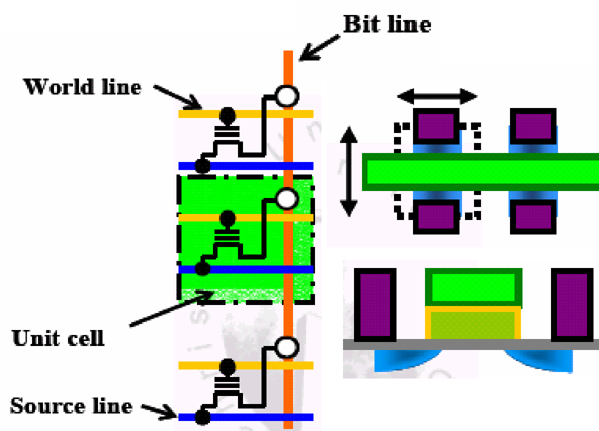


Fig. 79 The schematic cell array、layout view and cross section of the NOR architecture.
【中原大學：The Study of the novel NVM device(洪志學)】

	NOR	NAND
Advantages	Fast random access	Fast write and erase, higher density
Disadvantages	Slow write and erase	Slow random access Can't write single bytes
Applications	Code memory applications Cell phones, games	File memory applications Multi-media

NOR及NAND Flash比較

	NOR Flash(Code)	NAND Flash(Data)
儲存資料格式	程式碼	資料
資料存取方式	隨機存取	串列存取
讀取速度	快	慢
抹除速度	慢	快
寫入壽命	10萬次	100萬次
寫入速度（小筆資料）	快	慢
寫入速度（大筆資料）	慢	快
cell size	大	小
cell cost	高	低
耗電量	高	低
主流容量	64Mb	256Mb
主要應用	手機、PC、STB、DVD player	DSC、照相手機、MP3 player

S資料來源：台証整理

Fig. 80 NOR and NAND comparison.
【中原大學：The Study of the novel NVM device(洪志學)】

5.4 The type of Flash

The floating gate device conception was firstly published by D.Kahng and S.Sze. There are two insulator layers and the floating gate between the control gate and substrate in MIMIS. In MIMIS, the threshold voltage can be shifted by using the high failed effects to enhance electrons (or holes) trapped in the floating gate.

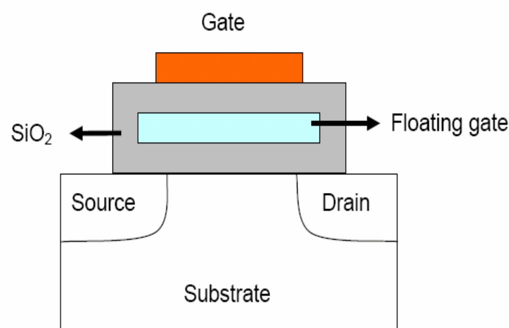


Fig. 81 Floating gate unit memory structure drawing

【聯合大學：A Study of Device and Reliability Measurements in the 0.25um Split Gate Flash Memory(張逸凡)】

The cross section of Flash memory that was presented by Intel in 1988 and named ETOX (EPROM Tunnel Oxide). The program and erase mechanism of ETOX are CHE injection and FN tunneling respectively.

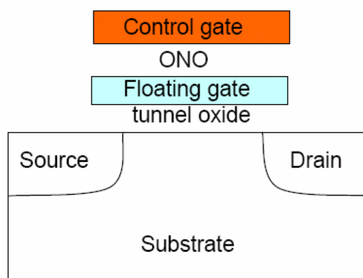


Fig. 82 ETOX unit memory structure drawing

【聯合大學：A Study of Device and Reliability Measurements in the 0.25um Split Gate Flash Memory(張逸凡)】

The cross section of Flash memory that was presented by W.L.Warren in 1997 and named Proton cell memory .It applications form Space and Military SONOS has the better scaling capability than that of floating gate device. And it can be scaled down beyond 0.18um. By applying the nitride layer instead of

floating gate, Sonos has low pinhole density, which induced leakage and longer retention time. SONOS can also achieve the low-power and low-voltage performance because it can be applied lower voltage to program and erase.

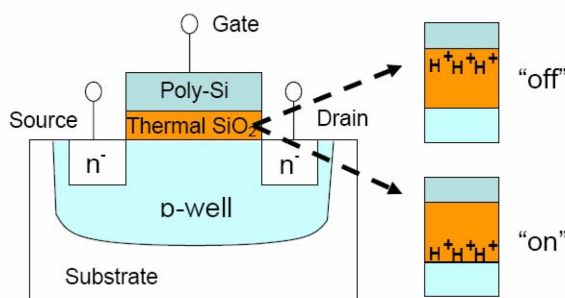


Fig. 83 Proton unit memory structure drawing

【聯合大學：A Study of Device and Reliability Measurements in the 0.25um Split Gate Flash Memory(張逸凡)】

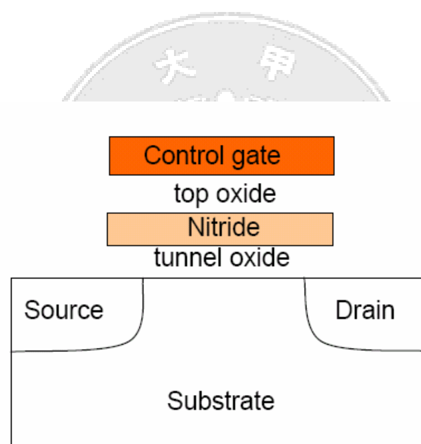


Fig. 84 SONOS unit memory structure drawing

【聯合大學：A Study of Device and Reliability Measurements in the 0.25um Split Gate Flash Memory(張逸凡)】

The other type of the floating gate memories is the split gate device. The schematic cross section of a split gate memory device is shown in Fig. 84. The channel is separated into two parts which are controlled by control gate and floating gate respectively. The programming mechanism of the split gate devices is the high efficiency drain-side channel hot electrons injection. A high voltage is applied on to control gate and the drain site. The erasing mechanism of the split gate devices is Fowler-Nordheim tunneling. A high electric field that pulls the electrons out of floating gate will be created along the tip of the floating gate near the control gate.

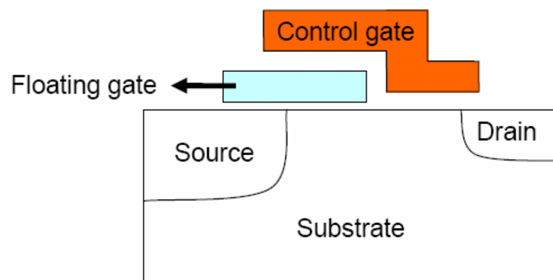


Fig. 85 Split gate unit memory structure drawing

【聯合大學：A Study of Device and Reliability Measurements in the 0.25um Split Gate Flash Memory(張逸凡)】

	Stacked Gate	**Split Gate**
Program Method	Channel Hot Electron Injection or FN tunneling	Channel Hot Electron Injection
Erase Method	FN tunneling	FN tunneling
Program Efficiency	Low	High

Fig. 86 Stacked gate and split gate comparison

【聯合大學：A Study of Device and Reliability Measurements in the 0.25um Split Gate Flash Memory(張逸凡)】

The single electron transistor or SET is type of switching device that uses controlled electron tunneling to amplify current. A SET is made from two tunnel junctions that share a common electrode. A tunnel junction consists of two pieces of metal separated by a very thin (~1 nm) insulator. The only way for electrons in one of the metal electrodes to travel to the other electrode is to tunnel through the insulator. Since tunneling is a discrete process, the electric charge that flows through the tunnel junction flows in multiples of e, the charge of a single electron.

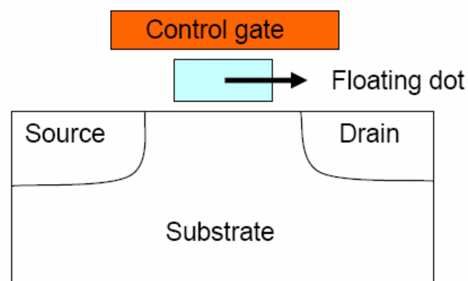


Fig. 86 Single electron / nano-point unit memory structure drawing

【聯合大學：A Study of Device and Reliability Measurements in the 0.25um Split Gate Flash Memory(張逸凡)】

5.5 Programming and Erasing

CHEI and FN tunneling are two main programming mechanisms of NVM device, CHEI is a higher-current programming operation than FN tunneling because the power consumptions of CHEI will be high. FN tunneling has the advantages of low current and potentially higher endurance, but the disadvantage of needing higher voltages in the memory array than CHEI.

F-N tunneling and BTBT are two main erasing mechanisms of n-channel NVM devices .The electrons in the floating gate are injected into the source and substrate by F-N tunneling method. BTBT induced hot hole injection is used as the erasing method of the NOE NVM device.

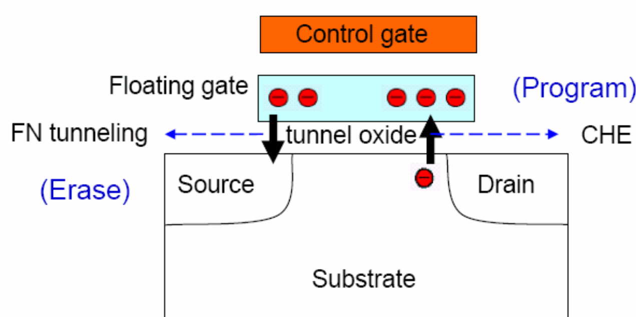


Fig. 87 Programming and erasing unit memory structure drawing

【聯合大學：A Study of Device and Reliability Measurements in the 0.25um Split Gate Flash Memory(張逸凡)】

The device threshold voltage will be shifted to different state. To distinguish whether the charge stored in floating gate or not, the logical "1" or "0", is therefore defined by defecting threshold voltage or drain current.

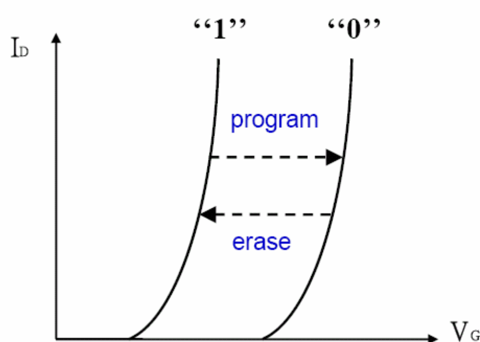


Fig. 88 Program: threshold voltage ↑:(0)

Erase : threshold voltage ↓:(1)

【聯合大學：A Study of Device and Reliability Measurements in the 0.25um Split Gate Flash Memory(張逸凡)】

5.6 Band to Band Tunneling Injection

Band to Band tunneling is an effect to be avoided in MOSFET design to reduce the off-state current. However, it can be advantageous as low-voltage programming and erasing mechanisms in NVMs devices. Band to Band is formed and higher than the energy gap of the semiconductor while the surface electric field is close to 1MV/cm. In this condition, a significant current flow can occur due to the tunneling of electrons from the valence band into the conduction band in n-channel devices. Electrons are collected by the drain, and holes are redirected to the surface and the substrate, thus the leakage current is generated. Lateral electric field does not allow the inversion layer to be generated, and this leads the space charge region in deep region, sweeping all the free carriers. This substrate current depends mainly on the vertical electric field in the oxide.

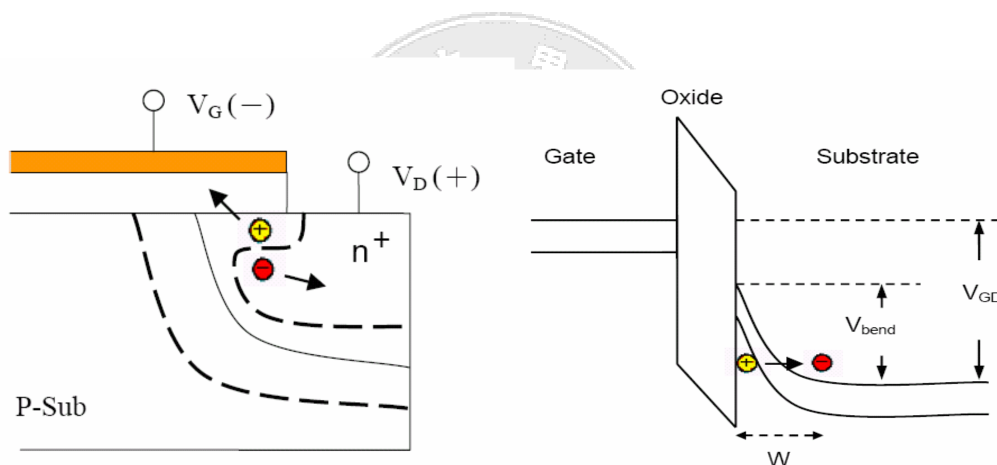


Fig. 89 Band to Band Tunneling Injection

【聯合大學：A Study of Device and Reliability Measurements in the 0.25um Split Gate Flash Memory(張逸凡)】

5.7 Fowler-Nordheim Tunneling Injection

The tunneling is a kind of quantum-mechanical process which a carrier can pass through a forbidden region. As the down-scaling of the device size continues into ultra thin gate oxides. There are two main types of tunneling including "Fowler-Nordheim Tunneling" and "Direct Tunneling". These two tunneling mechanisms both increase the standby power consumption due to their high static gate current. Once the oxide layer thickness is thinner to 4nm or less, such "Direct Tunneling" is likely to occur in thin oxide at a low field. The main difference between "Direct Tunneling" and "F-N tunneling" is their transport path of electrons tunneling into the gate. The direct tunneling gate current at low gate bias is a considered as "cold" carrier gate current. For ultra-thin oxide, electrons can directly tunnel through the forbidden energy gap from the inverted silicon surface to the gate without the need of entering the oxide conduction band. For that oxide thickness of 30 nm or less, it is not useful for NVMs because charges placed on a gate by this process find themselves equally possible to stay or leave, which is related to the data retention issues.

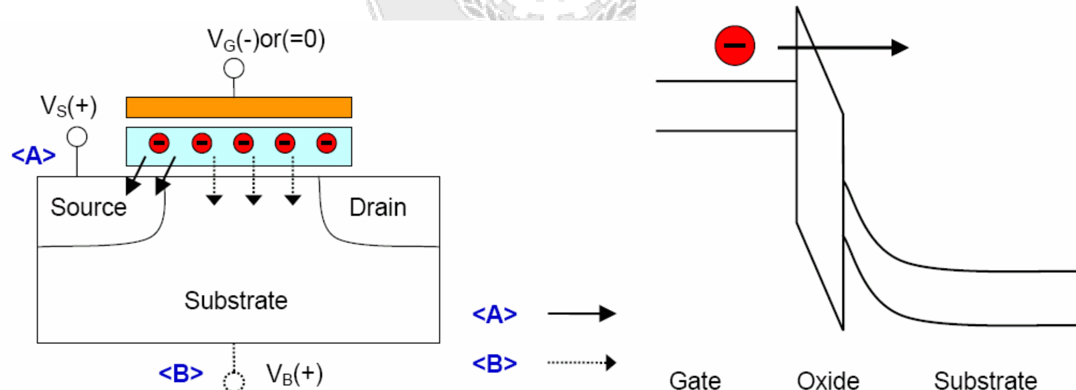


Fig. 90 Fowler-Nordheim Tunneling Injection

【聯合大學：A Study of Device and Reliability Measurements in the 0.25um Split Gate Flash Memory(張逸凡)】

5.8 Channel hot electron Injection

If the device dimensions are reduced and the supply voltage remains constant, the lateral electric field in the channel increases. The hot carrier effect and its characterization on MOSFET device have been found and studied since the late 1970s. As the MOSFET size shrinking into submicron regime, the hot-carrier effect becomes more and more dominant. Hot carriers, generation in MOSFETS takes place under a strong inversion. The high lateral electric field in the channel causes the charges in the inversion-layer to be accelerated. While a high drain to source bias voltage and a high control gate voltage are applied, the pinch off point occurs and is close to the drain junction edge of the transistor channel where the vertical electric filed starts to rise rapidly. At the pinch off point of the MOSFET, toward the drain junction edge, the electric field starts to rise rapidly. This rising electric field causes the carriers to gain energy from the field. There are two main phenomena related to hot-carrier degradations. The one is that electrons with sufficient energy can create additional channel carriers by impact ionization in the channel region. These generate secondary electron-hole pairs. Hot carrier effects also introduce a number of harmful device phenomena, such as the degradations of the threshold voltage, linear region trans conductance , sub threshold slope, saturation current, and gate oxide quality. The hot carriers injected into the gate oxide create many damages.

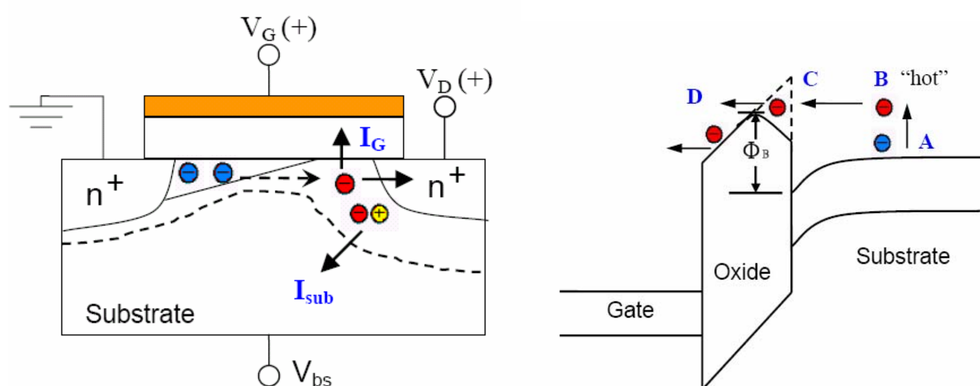


Fig. 91 Channel hot electron Injection

【聯合大學：A Study of Device and Reliability Measurements in the 0.25um Split Gate Flash Memory(張逸凡)】

5.9 The “Read” operation of SONOS

Novel features of the SONOS are the read operations. The conventional technique of reading is to apply read voltage to the gate and drain and to ground the source. Physical two-bit storages in charge trapping NVM devices are based on the unique localized charge trapping characteristic. Two bits per cell operations can be realized by using a novel read method that was proposed by Boaz Eitan of Saifun. This is similar to the method of programming but the lower voltage is required during reading than those during programming. The conventional NVM typically works well with programming and reading in the same current flow direction. In a floating gate programmed device, the threshold voltage is high for the entire channel and the process of reading becomes symmetrical. In the two-bit NVM devices, bit-1 and bit-2 allow two read directions which are namely “forward” read and “reverse” read depending on their current flow of reading. Thus, the process of reading becomes asymmetrical NOE NVM utilizes this asymmetrical reading to accomplish the two-bit operation.

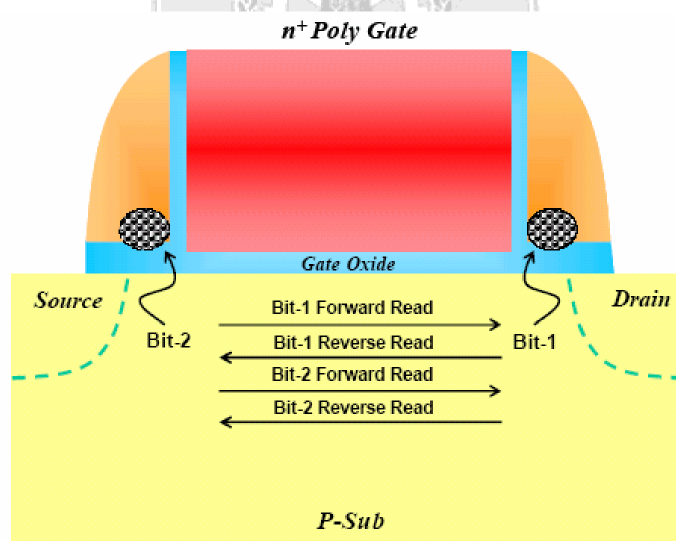


Fig. 92 The read directions of the NOE NVM device

【中原大學：The Study of the novel NVM device(洪志學)】

5.10 Future development

5.10.1 MRAM memory and FeRAM

Magnetic core memories were used in early mainframe computers. The modern magnetic RAM is primarily a development of the last two decade. Magnetization is a result of the electrons spin in a ferromagnetic metal such as iron, cobalt and nickel. The magnetic field applied on MRAM magnetizes these materials. MRAM store information as the orientation of magnetization of a ferromagnetic region. FeRAM is currently one of several "advanced" non-volatile memory (NVRAM) technologies that are attempting to gain acceptance as an alternative to flash by avoiding its key weaknesses – high program and erase voltages, slow programming speed, write-erase endurance that is limited to ~105 cycles. Compared to its primary competitors among the new NVRAM technologies, MRAM and PRAM, FeRAM is more mature with volume production at Fujitsu beginning in 1999.

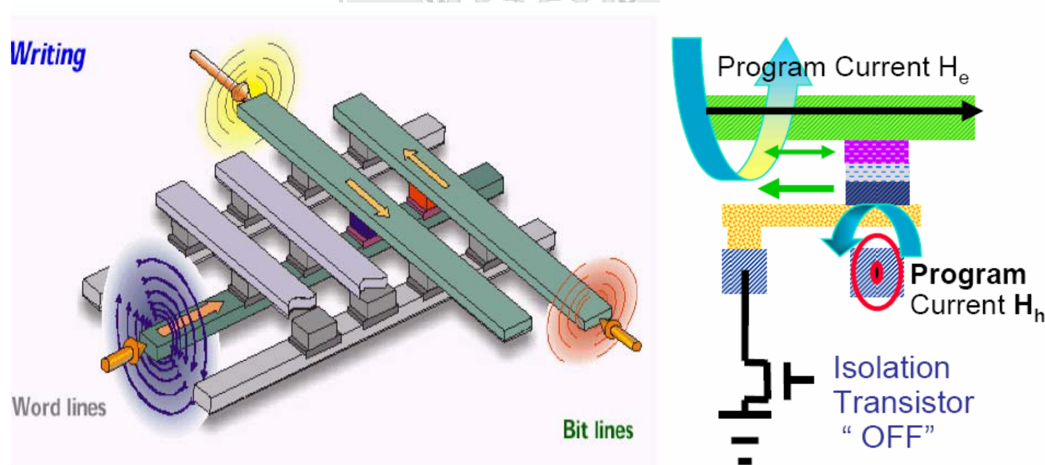


Fig. 93 FeRAM structure and operation element

【奈米電子元件技術組電子所：非揮發性記憶體(NVM)、相變化記憶體(PCM)(高明哲)】

Ferro electric memories have also been developed for many years. The ferroelectric RAM cell stores data in a capacitor which uses a ferroelectric film as the dielectric. Once the voltage is applied on of the crystal cells in the ferroelectric film. The polarization effect with two net stable states when the applied voltage is removed.

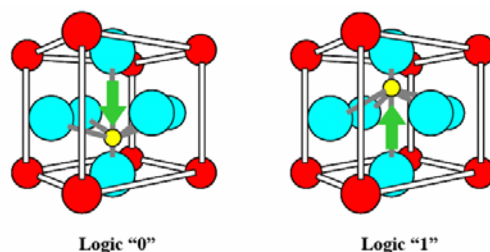


Fig. 94 Logic element

【電子月刊，鐵電記憶元件特輯，April,2002】

5.10.2 Phase Change Memory

Phase change random access memory (PCRAM) is one of the candidates for next generation RAMs and could be competitive with Flash memory due to its amazing characteristics, such as high-density, high-speed, non-volatility and scalability. However, several problems remain to be solved before commercialization of PCRAM. One of the biggest problems is the quite high reset current during the operation. There were many proposals to reduce the reset current. For example, N-doping into Ge2Sb2Te5 was found to successfully decrease the reset current and becomes a suitable chalcogenide material in PCRAM due to its higher electrical resistivity in the crystalline phase. Special device designs were also reported to improve this property, such as an edge-contact type cell, μ Trench PCRAM cell, and lateral PCRAM cell and phase change line memory. Furthermore, it was also reported that by inserting a high resistive heating layer (~10 nm) between the bottom electrode and the phase-change material could successfully decrease the operation current. The simulation results suggested that a suitable inserted heating layer should possess an electrical resistivity (ρ elec) higher than 0.1 Ω cm, and with thermal conductivity κ and specific heat as low as those of phase-change material, such as Ge2Sb2Te5. Therefore, a device with a highly resistive TiON layer (~7 nm) which was sandwiched between the TiN bottom electrode and Ge1Sb2Te4 revealed lower reset and set voltages than those without. It is believed that the selection of the right materials as inserted heating layers could be an excellent way to facilitate the commercialization of PCRAM.

Earlier study showed that interfacial instability including the inter-diffusion between the chalcogenide material and the bottom electrode is one of the main reasons for the low cycle life of PCRAM cells. Ternary systems of the type TM-Si-N (TM = Ti, Ta, Mo or W) have shown remarkable barrier performance in semiconductor devices.

Specifically, many researches were done on Ti-Si-N films because of their outstanding barrier performance in Cu metallization. Therefore focused researches of Ti-Si-N films were on the deposition and resultant characteristics of such films, while others were on the formation of nano-composite structures and the related mechanical properties.

The purpose of this study was to contribute a useful heating layer, which would in the meantime also act as a diffusion barrier for PCRAM of a long cycle life. The material was based on Si-rich SiTiNx composition with a high electrical resistivity falling in the range of simulation proposal. Such films were expected to be different from the highly conductive Ti-rich Ti-Si-N for interconnects in Cu processing.

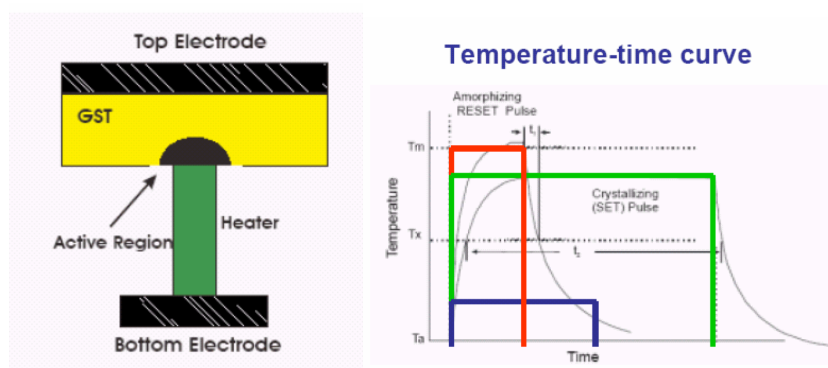


Fig. 95 Phase Change Memory structure and Temperature-Time curve

【奈米電子元件技術組電子所：非揮發性記憶體(NVM)、相變化記憶體(PCM)(高明哲)】

5.11 Conclusion

Silicon-oxide-nitride-oxide-silicon (SONOS) becomes more and more attractive because of its high compatibility with existing CMOS logic processes and simplicity in device structures. Recently, the two-bit operation of SONOS which used channel hot electron injection to program and hot hole enhanced injection to erase attract more and more practical applications. It can easily achieve cost reduction simply by doubling the bit counts in the same area. However, its reliability issues are considered as challenges to be solved in the near future. Because of the Frenke-Poole emission and oxide trap assisted tunneling, the program-state threshold voltage has a negative shift. And the net positive charge in the bottom oxide assisted the substrate electron injecting cause the erase-state threshold voltage has a positive shift. It is not easy to predict that how the flash will be developed in the future，but it is necessary to developed it to become tiny, fast, and a big capacity.

Chapter 6 Nanowires

6.1 Abstract

Semiconductor nanowires (NWs) represent a unique system for exploring phenomena at the nanoscale and are also expected to play a critical role in future electronic and optoelectronic devices. Here we review recent advances in growth, characterization, assembly and integration of chemically synthesized, atomic scale semiconductor NWs. We first introduce a general scheme based on a metal-cluster catalyzed vapor–liquid–solid growth mechanism for the synthesis of a broad range of NWs and nanowire heterostructures with precisely controlled chemical composition and physical dimension. Such controlled growth in turn results in controlled electrical and optical properties. Subsequently, we discuss novel properties associated with these one-dimensional (1D) structures such as discrete 1D subbands formation and Coulomb blockade effects as well as ballistic transport and many-body phenomena. Room-temperature high-performance electrical and optical devices will then be discussed at the single- or few-nanowire level. We will then explore methods to assemble and integrate NWs into large-scale functional circuits and real-world applications, examples including high-performance DC/RF circuits and flexible electronics. Prospects of a fundamentally different 'bottom-up' paradigm, in which functionalities are coded during growth and circuits are formed via self-assembly, will also be briefly discussed.

6.2 Introduction

Great advances in integrated circuit technologies have been accomplished during the past four decades that resulted in electronic devices with higher device density, faster clock rate and lower power consumption. However, as the devices reach deep sub-100 nm scale, conventional scaling methods which maintain the device's basic structure while shrinking its size face increasing technological and fundamental challenges. For example, device size fluctuations will result in a large spread in device characteristics at the nanoscale, affecting key parameters such as the threshold voltage and on/off current. Increasing demand on the resolution of the equipment and

expenses of building and operating the facilities also pushes the traditional approach towards its practical limit and hinders device scaling from reaching true atomic level. To sustain the historical scaling trend beyond CMOS, novel one-dimensional (1D) structures, including carbon nanotubes (CNTs) and semiconductor nanowires (NWs), have been proposed as the active components (as well as interconnects) in future nanoscale devices and circuits. In this case, the critical device size is defined during the growth (chemical synthesis) process and can be controlled with atomic scale resolution. To date, great efforts and progress have been made in the field of CNTs, although CNT based applications are still hindered by difficulties to produce uniform, semiconducting nanotubes. On the other hand, semiconductor NWs can be prepared with reproducible electronic properties in high-yield, as required for largescale integrated systems. Furthermore, the well-controlled NW growth process implies that materials with distinct chemical composition, structure, size and morphology can be integrated. Such an ability to build specific functions into the system during growth may in turn lead to bottom-up assembly of integrated circuits, which offers the potential of parallel production of massive number of devices with similar material and electrical/optical properties. Drastically different from the ‘top-down’ paradigm commonly used in today’s semiconductor industry, this ‘bottom-up’ paradigm, analogous to the way that nature works, may prove to be a suitable solution to the technological challenges as devices approach atomic size. From a fundamental physics point of view, the low dimensional nanowire structure is an ideal platform to probe properties which may be inaccessible or hard to achieve in larger devices, due to the reduced device size and ideal material properties. For example, discreteness of electrons comes into play when the Coulomb energy associated with the addition of an individual electron becomes larger than the thermal energy; 1D quantum wires and zero-dimensional quantum dots (QDs) form when the relevant device size is comparable to the de Broglie wavelength of the carriers. As a result, the electrical and optical properties in these nanoscale devices are determined not only by the materials composition but can also be tailored by the specific device geometry.

6.3 Growth of NWs

6.3.1 The vapor–liquid–solid growth method

Semiconductor NWs are generally synthesized by employing metal nanoclusters as catalysts via a vapor–liquid–solid (VLS) process (Fig. 96). In this process, the metal nanoclusters are heated above the eutectic temperature for the metal–semiconductor system of choice in the presence of a vapor-phase source of the semiconductor, resulting in a liquid droplet of the metal/semiconductor alloy. The continued feeding of the semiconductor reactant into the liquid droplet supersaturates the eutectic, leading to nucleation of the solid semiconductor. The solid–liquid interface forms the growth interface, which acts as a sink causing the continued semiconductor incorporation into the lattice and, thereby, the growth of the nanowire with the alloy droplet riding on the top. The gaseous semiconductor reactants can be generated through decomposition of precursors in a chemical vapor deposition (CVD) process or through momentum and energy transfer methods such as pulsed laser ablation or molecular beam epitaxy (MBE) from solid targets. So far, CVD has been the most popular technique. In CVD–VLS growth, the metal nanocluster serves as a catalyst at which site the gaseous precursor decompose, providing the gaseous semiconductor reactants. In the case of SiNW growth (Fig. 96), silane (SiH4) and Au nanoparticles are normally used as the precursor and catalysts, respectively. Besides group IV materials, compound III–V and II–VI NWs have also been produced with the VLS method, in which pseudo binary phase diagrams for the catalyst and compound semiconductor of interest are employed. In the compound semiconductor case, metal-organic chemical vapor deposition (MOCVD) or pulsed laser ablation are typically used to provide the reactants. There are two competing interfaces during nanowire growth, the liquid/solid interface between the eutectic and the nanowire and the gas/solid interface between the reactants and the exposed surface of the growing nanowire. Precipitation through the first interface results in the VLS growth and axial elongation of the nanowire, while dissociative adsorption on the second interface results in vapor–solid growth and thickening in the radial direction. Either mechanism can be dominating in an actual growth process, depending on the detailed growth condition such as the pressure, flow rate, temperature, reactant species and background gases that

are by-products of growth reactions. For example, in the abovementioned SiNW growth process, low temperature growth can reduce the rate of direct thermal dissociation of silane; hence, axial nanowire growth is favored. Hydrogen has also been found to mitigate radial growth through suppression of either the adsorption of the reactants by terminating the Si surface or of the dissociation of silane. The use of H2 as the carrier gas also passivates the NWsurface in a manner similar to that observed in thin-film growth and reduces roughening along the NW. Uniform NWs with negligible diameter variation can thus be achieved through careful control of the growth conditions, including the employment of local heaters to reduce uncontrolled decomposition of silane. On the other hand, tapered NWs are products from simultaneous growth in both the axial and radial directions and are generally not desirable for most electrical and optical applications. In the CVD–VLS growth process the diameter of the nanowire is determined by that of the starting nanocluster, and uniform, atomic-scale NWs can be obtained in a well controlled growth process as nanoclusters with diameters down to a few nanometers are now commercially available. Wu et al reported growth of uniform SiNWs with diameters down to 3 nm using SiH4 as the precursor and H2 as the carrier gas. Wu performed detailed high-resolution transmission electron micrography (HRTEM) studies on these SiNWs and observed that the NWs are single-crystalline with little or no visible amorphous oxide even at this scale. The resulting SiNWs show narrow size distributions of 13.2±1.7 nm, 5.9±1.1 nm, and 4.6 ± 1.2 nm, respectively when gold nanoclusters of diameters of 10 (9.7 ± 1.5) nm, 5 (4.9 ± 0.7) nm, and 2 (3.3 ± 1) nm are used. The increase in the NW diameters compared with those of the starting nanoclusterswas attributed to the supersaturation of silicon in gold nanoclusters during the formation of the liquid droplet prior to nucleation, an effect observed previously with in situ observations of the growth of germanium NWs.

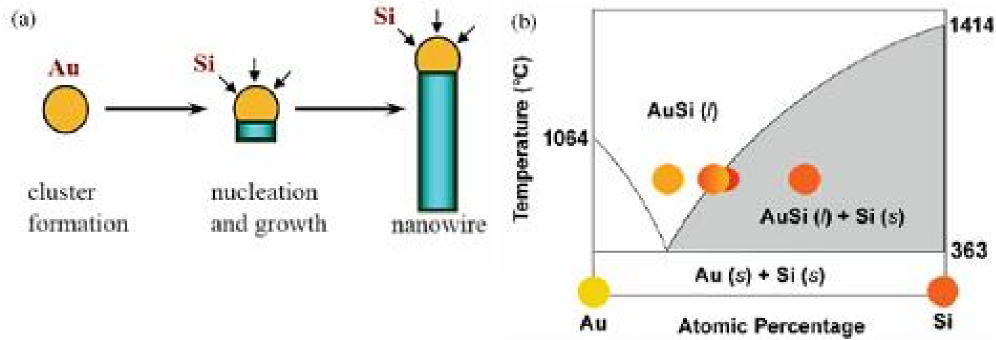


Fig. 96 Schematic of VLS growth of Si nanowires (SiNWs). (*a*) A liquid alloy droplet AuSi is first formed above the eutectic temperature (363 ◦C) of Au and Si. The continued feeding of Si in the vapor phase into the liquid alloy causes oversaturation of the liquid alloy, resulting in nucleation and directional nanowire growth. (*b*) Binary phase diagram for Au and Si illustrating the thermodynamics of VLS growth.

【Wagner R S 1970 Whisker Technology (New York: Wiley)】

6.3.2 Nanowire heterostructures

Compared with nanostructures fabricated from other approaches such as vapor–solid growth or solution based liquid–solid growth, the VLS process offers one key advantage—heterostructures can be achieved at the individual device level in a controlled fashion. Both axial heterostructures (Fig. 97(c) and (e)), in which sections of different materials with the same diameter are grown along the wire axis , and radial heterostructures (Fig. 97(d) and (f)), in which core/shell and core/multi-shell form along the radial direction , have been realized on VLS–CVD grown NWs. To understand the rational formation of nanowire heterostructures within the context of the VLS method, consider the possible effects of a change in reactant vapor once nanowire growth has been established (Fig. 97). If vapor decomposition/adsorption continues exclusively at the surface of the catalyst nanocluster site, crystalline growth of the new semiconductor will continue along the axial direction (Fig. 97(c)). On the other hand, if the decomposition of the new vapor/reactant on the surface of the semiconductor nanowire cannot be neglected, a shell of material will grow on the original nanowire surface (Fig. 97(d)). Repeated changing of reactants in a regime favoring axial growth will lead to the formation of a nanowire superlattice, as shown in Fig. 97(e), while changing reactants in a radial-growth regime will result in core-multi-shell radial structures, as shown in Fig. 97(f). It is important to mention that there are few constraints on the

composition of the shell growth; any material suitable for planar film deposition can be deposited on the surface of a nanowire, and crystalline radial heteroepitaxy can be achieved as the nanowire surface is crystalline.

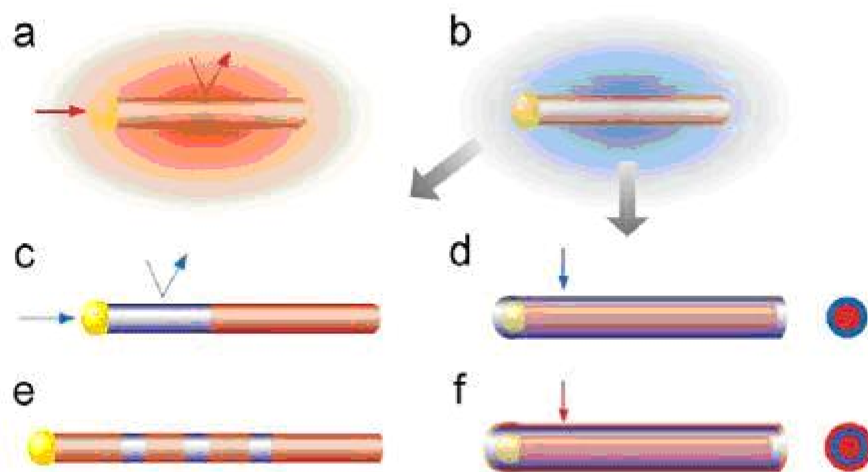


Fig. 97 Nanowire heterostructure synthesis. (*a*) Preferential reactant incorporation at the catalyst (growth end) leads to 1D axial growth. (*b*) A change in the reactant leads to either (*c*) axial heterostructure growth or (*d*) radial heterostructure growth depending on whether the reactant is preferentially incorporated (*c*) at the catalyst or (*d*) uniformly on the wire surface. Alternating reactants will produce (*e*) axial superlattices or (*f*) core-multi-shell structures.

【Kong Y C, Yu D P, Zhang B, Fang W and Feng S 2001 Appl. Phys. Lett. 78 407】

6.3.2.1 Radial nanowire heterostructures

Radial core / shell heterostructures can be achieved if dissociation of the reactants is promoted at the grown nanowire surface (Fig. 97(d)), analogous to the layered growth of planar heterostructures. Compared with NWs in the simple homogeneous form, core/shell heterostructure NWs offer better electrical and optical properties as they can now be tailored through band structure engineering.

6.3.2.2 Axial nanowire heterostructures

Unlike radial heterostructures in which the shell growth does not involve reaction with the nanocluster catalyst, axial nanowire heterostructures can be obtained by alternative introduction of vapor phase reactants that react with the same nanocluster catalyst, as illustrated in Fig. 97(c) and (e). A critical requirement of the axial nanowire heterostructure growth is then that a single

nanocluster catalyst can be found which is suitable for growth of the different components under similar conditions.

6.3.3 Growth of metal oxide NWs

Besides the VLS approach, a simple thermal evaporation/ vapor transport deposition approach has also been shown to be effective in growing 1D structures, in particular metal oxide (e.g. ZnO, In2O3 and SnO2) NWs. Such NWs have been studied in applications ranging from optoelectronics devices, field-effect transistors, ultra-sensitive nanoscale gas sensors and field emitters. In particular, ZnO NW shave attracted a lot of interest due to the large exciton binding energy (60meV), high electromechanical coupling constant and resistivity to harsh environment. The first attempt to produce ZnO NWs was based on an electrochemical method using anodic alumina membranes (AAM). Later on, high-density, ordered ZnO nanowire arrays were obtained using AAM in a vapor-deposition process. However, the AAM approach is typically limited to generating polycrystalline NWs. To produce singlecrystalline 1D ZnO nanostructures, a number of methods have been explored such as thermal evaporation / vapor transport deposition, hydrothermal process, MOCVD, pulsed laser deposition and MBE. Among all methods used to grow metal oxide NWs, thermal evaporation / vapor transport deposition has gained the most popularity. The thermal evaporation technique is based on a simple process in which source materials in the condensed or powder form are first vapourized at an elevated temperature; the resulting materials in vapor phase then condense under the right conditions (temperature, pressure, atmosphere, substrate, etc) to form the desired product. The processes are usually carried out in a setup as shown in Fig. 98, which includes a horizontal tube furnace, a quartz or alumina tube, gas supplies and control system. Single-crystalline ZnO NWs grown with the thermal evaporation method (referred also as the physical vapor deposition method) were first reported in 2001, with an average diameter of about 60 nm. In 2002, Yao et al reported mass production of ZnO NWs, nanoribbons and needle-like nanorods by thermal evaporation of ZnO powders mixed with graphite. Yao found that temperature was the critical experimental parameter for the formation of different morphologies of ZnO nanostructures. Banerjee et al succeeded in producing grams of ZnO NWs via thermal evaporation of ZnO powder in a tube furnace at high temperatures. The graphite flakes were found to be the key.

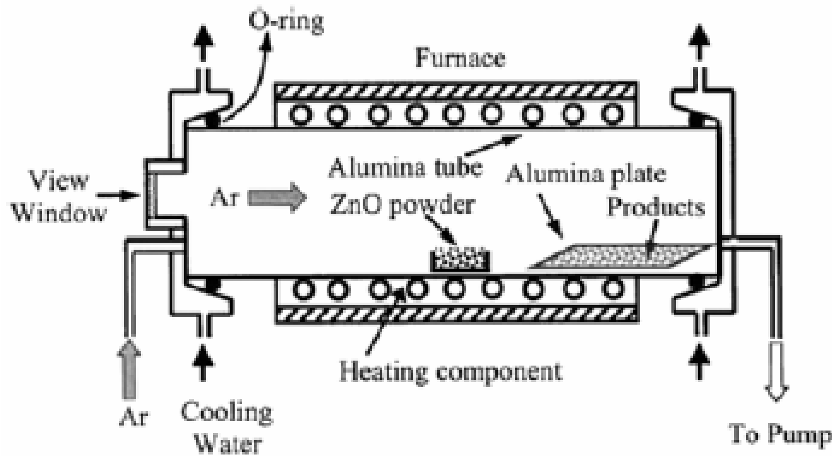


Fig. 98 Schematic diagram of the horizontal tube furnace for growth of ZnO nanostructures. Reprinted with permission from .

【Qian C, Kim F, Ma L, Tsui F, Yang P and Liu J 2004 J. Am. Chem. Soc. 126 1195】

6.4 Nanowire electronic devices

6.4.1 Field-effect transistor devices

Silicon NWs (SiNWs) have been most extensively studied partly due to the dominance of Si devices in the semiconductor industry and partly due to the well-developed recipes to grow SiNWs with controlled size and doping level. In typical device geometry, the SiNWs are first transferred into liquid suspension after growth via gentle sonication, then dispersed on a degenerately doped Si substrate with a SiO2 overgrowth layer, as shown in Fig. 99. Devices in the form of field-effect transistors can then be studied after source–drain electrode formation which is normally carried out by e-beam or photo-lithography, with the degenerately doped Si substrate serving as the back gate. Unlike conventional MOSFETs in which the source / drain contacts are formed by degenerated doped Si, metal contacts are commonly used in a nanowire device. In this regard, a nanowire FET device is essentially a Schottky barrier device. Typically positive Schottky barriers are observed at the metal/semiconductor interface due to the combined effect of metal work function and Fermi level pinning by surface states. As a result, the device performance is to a large degree affected by the contact properties. For example, Cui et al observed that after thermal annealing which was believed to improve the source / drain contacts, the average transconductance of the

SiNW devices increased from 45 to 800 nS and the deduced average mobility μ increased from 30 to 560 cm2 $(V\ s)^{-1}$. In Cui's study, boron-doped (p-type) SiNWs with diameters in the 10–20 nm range were used. The nanowire FETs were fabricated using Ti S/D contacts, and transport characteristics were studied as a function of annealing. Ti was used since it is known that Ti can form a stable conducting silicide with a low Schottky barrier height on p-type silicon. Fig. 99(A) shows the current (I) versus source– drain voltage (V_{sd}) behavior of a typical Ti-contacted SiNW device before and after thermal annealing. In general, the I–V_{sd} curves become more linear and symmetric, and the transport behaviour becomes more stable after annealing, with the measured conductance increasing by 3-fold. To characterize the reproducibility of these observations, similar measurements were made on over 50 devices. These results are summarized in a histogram showing the frequency that different values of two-terminal resistance were observed (Fig. 100(B)). Before annealing, the resistance shows a large distribution ranging from ~MΩ to larger than GΩ with an average of 160MΩ. In contrast, the resistance after annealing has a narrower distribution of 0.1–10MΩ with an average of 0.62MΩ; that is, a 260 fold improvement in the two-terminal conductance. The increased two-terminal conductance and stability can be attributed in part to better metal SiNW contacts, although passivation of defects at Si–SiOx interface, which can occur during annealing, may also contribute to the observed enhancements. The mobility of the nanowire devices can be extracted from the measured tranconductance gm = dI/dVg. At low biases, the following relationship governs transport in an ideal FET device:

$$g_m = \frac{\mu C}{L^2} V_{sd} \quad \text{equation (1)}$$

Where C is the total gate capacitance and L is the channel length of the device. On the other hand, the measured transconductance g_{ex} with finite source/drain contact resistances is reduced from its intrinsic value gin to

$$g_{ex} = \frac{g_{in}}{1 + g_{in} R_s + (R_S + R_d)/R_{in}} \quad \text{equation (2)}$$

Where R_s and R_d are, respectively, the source and drain contact resistance, and R_{in} is the intrinsic nanowire resistance. From equation (2), it is clear that contact resistances can greatly influence the performance of nanowire transistors, and the extracted mobility using equation (1) may not reflect the true intrinsic mobility of the device. For example, in the extreme case when Rs >>1/gin, g_{ex} ~1/Rs and becomes independent of gin. Such a scenario can occur either when the contacts are poor or when high performance transistors

are desired such that even a small Rs is unfavourable due to the large gin. Zheng et al carried out detailed studies on SiNW FETs with a geometry similar to that illustrated in Fig. 99. The SiNWs used in this study were n-type (doped with phosphorus). As expected, the nanowire devices exhibited depletion mode n-type MOSFET behaviour, as illustrated in Fig. 101. Interestingly, Zheng observed that the heavily doped devices (Si/P = 500) exhibit an apparent larger transconductance compared with the lightly doped devices (Si/P = 4000), at the same device geometry and bias voltage conditions. This observation, however, contradicts the predictions of equation (1), as the heavily doped NWs would suffer from increased impurity scattering and possess a lower mobility, as previously observed in bulk materials.

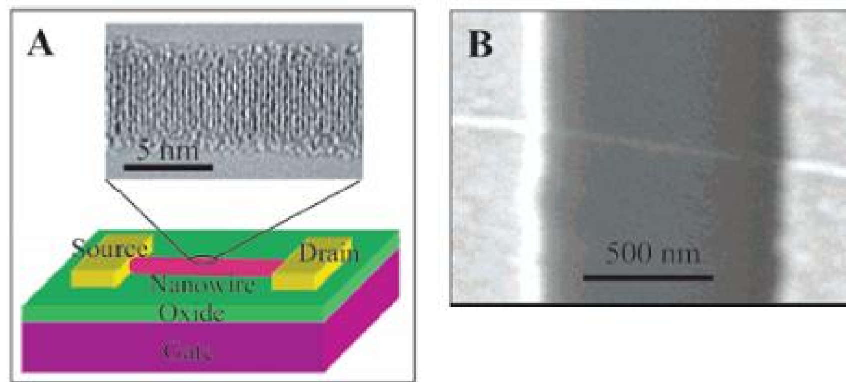


Fig 99 (A) Schematic of a SiNW FET showing metal source and drain electrodes. (Inset) HRTEM of a 5 nm diameter SiNW. (B) Scanning electron micrograph of a SiNW FET device.

【Cui Y, Zhong Z, Wang D, Wang W U and Lieber C M 2003 Nano Lett. 3 149】

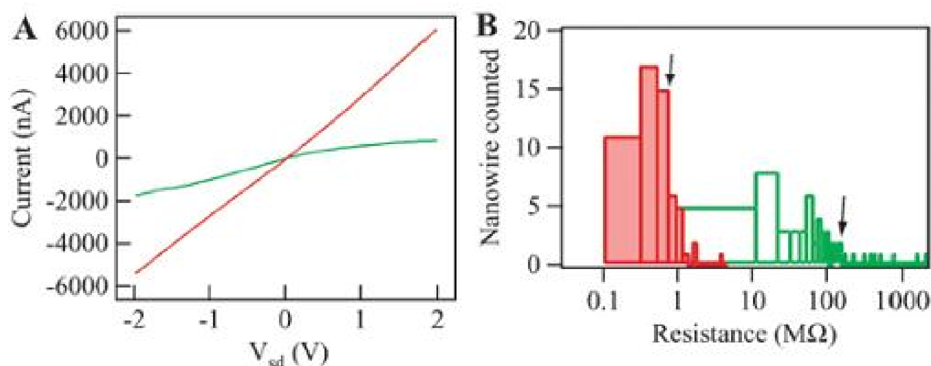


Fig. 100 (A) I versus Vsd measured on the same SiNW before (green) and after (red) thermal annealing. (B) Histogram of Ti-contacted SiNW resistance determined from measurements before (open green bars) and after (filled red bars) contact annealing.

【Gambino J P and Colgan E G 1998 Mater. Chem. Phys. 52 99】

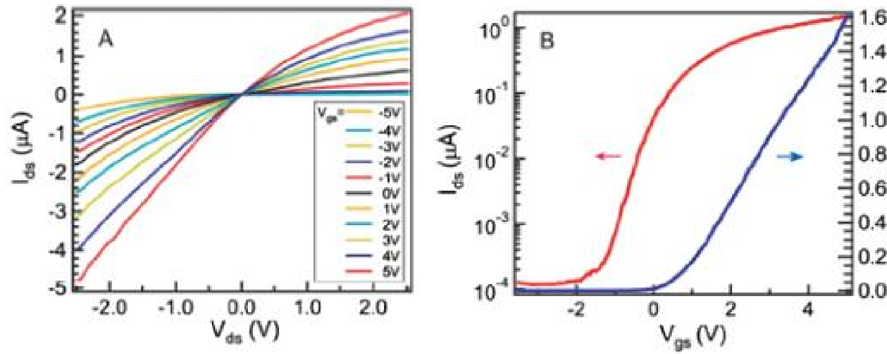


Fig. 101 Electrical transport in a lightly doped n-type SiNW device. (A) Ids versus Vds curves recorded at different Vg. (B) Ids versus Vg curve at Vds = 1V in linear (blue) and logarithmic scale (red), respectively.

【Gambino J P and Colgan E G 1998 Mater. Chem. Phys. 52 99】

6.5 Assembly and integration techniques

As can be seen in the case of Ge / Si core/shell NWs, the quasi-1D transport nature and clean material structure of the nanowire system result in superior device performance, compared with even state-of-the-art planar devices. However, the discussions so far are limited to the individual device level. To fully explore the potential of NW building blocks for integrated devices and circuits, efficient and scalable strategies are needed to assemble large amount of NWs into increasingly complex architectures. In this regard, two key gradients are involved in the large scale assembly and integration of nanowire devices. First, methods are needed to assemble NWs into highly integrated arrays with controlled orientation and spatial position. Second, approaches must be devised to assemble NWs on multiple length scales and to make interconnects between nano-, micro- and macroscopic worlds. To date, several different approaches have been adopted to address these issues and are briefly reviewed in this chapter.

6.5.1 Fluidic flow-directed assembly technique

The first successful demonstration of rational assembly of NWs was achieved with the electric field assembly technique developed by Duan et al, by noting that NWs tend to align with the direction of an applied electric field. Duan showed that individual wires can be positioned to bridge pairs of diametrically opposed electrodes and form a parallel array. Crossed nanowire structures can also be achieved by changing the direction of the electric field in a layer by layer fashion. However, electric field assembly suffers from several limitations, including (1) the need to pattern microelectrode arrays used to produce aligning fields and (2) the deleterious effect of fringing electric fields at the submicron length scales resulting in misalignment. To address theses issues, a simple, fluidic flow-directed assembly method was independently developed by the Lieber group at Harvard and the Yang group at UC Berkeley. In the fluidic flow-directed assembly method, nanowire alignment is achieved by passing a suspension of NWs through a microfluidic channel, for example, formed between a poly(dimethylsiloxane) (PDMS) mould and a flat substrate(Fig. 102(A). Virtually all NW scan be aligned along the flow direction at an adequate flow rate, leaving an array of parallel NWs assembled on the substrate surface within the microfluidic channel. The alignment can be readily extended to over hundreds of micrometres and is limited only by the size of the fluidic channel being used. The alignment of NWs within the channel flow can be understood within the framework of shear flow. Specifically, the channel flow near the substrate surface resembles a shear flow, and linear shear force aligns the NWs in the flow direction before they are immobilized on the substrate. The average NW surface coverage can be controlled by the flowduration. Huang found that the NW density increases systematically with the flow duration at a constant flow rate. For example, a flow duration of 30 min produced a density of about 250NWs per 100mmor an average NW–NW separation of 400 nm, and NW spacing on the order of 100 nm or less can be achieved with an extended deposition time. Using a layer-by-layer deposition process, more complex crossed NW structures can be obtained with the fluidic flow assembly approach (Fig. 102(B)). The layer-by-layer approach requires that the nanowire–substrate interaction is sufficiently strong so that sequential flow steps will not affect the existing patterns, a condition that can be achieved by modifying the substrate surface with proper functional chemical groups. For example, crossbar structures with high yield have been demonstrated by alternated flow in orthogonal directions in a two-step assembly process. The

fluid flow alignment technique offers several advantages compared with pervious attempts. First, it is an intrinsically parallel process without the need for patterned electrodes. Second, this approach is applicable for virtually any elongated nanostructure including CNTs and DNA molecules. Third, it allows for the directed assembly of geometrically complex structures by simply controlling the angles between flow directions in sequential assembly steps. For example, equilateral triangles have been assembled in a three-layer deposition sequence. Finally, since each layer is independent in the flow alignment process, a variety of homo- and hetero-junction configurations can be obtained by simply changing the composition of the NW suspension used in each step. However, controlled assembly of NWs with the fluidic flow method at larger scales (> centimetre) is less practical and remains to be demonstrated.

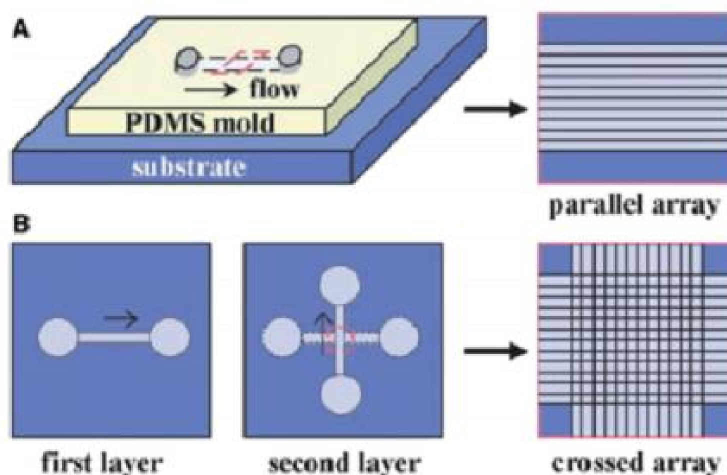


Fig. 102 Schematic of the fluidic flow alignment process. (A) NW assembly was carried out by flowing a NW suspension with a controlled flow rate for a set duration inside the channel formed between the PDMS mould and a flat substrate. (B) Multiple crossed NW arrays can be obtained by changing the flow direction sequentially in a layer-by-layer assembly process .

【Gambino J P and Colgan E G 1998 Mater. Chem. Phys. 52 99】

6.6 Nanowire circuits

6.6.1 NW crossbar circuits

Implementation of the nanowire devices in ultra-high density, large-scale application will likely in turn require the implementation of novel architectures. This includes both nano-architectures at the circuit level that link large numbers of devices with each other and with external systems to perform memory and/or logic functions as well as system architectures that allow the circuits to communicate with other systems and operate independently of their lowerlevel details. In particular, since traditional defect-free oriented processes will likely no longer be feasible at the molecular scale, the new architectures must be defect-tolerant. Reconfigurable architectures, particularly crossbar structures in which active devices are formed at the intersections when two sets of wires cross each other, have been demonstrated to possess desirable properties at both the nano-architecture as well as the system-architecture level. In an earlier proof-of-concept study, Duan et al and Huang et al have shown that prototype logic circuits can be achieved on crossed nanowire p/n junctions. In these studies, the cross-wire structures were achieved via flow alignment, and devices at the single to few NW levels were examined. To implement desired hierarchical patterning of arrays of aligned and crossed NWs at centimetre scale, Whang et al developed a technique in which locating individual NWs to the desired positions is no longer required. In Whang's approach, a monolayer of aligned NWs was produced first via the LB approach. Photolithography was then used to define a pattern over the entire substrate surface which sets the array dimensions and array pitch. Finally, NW soutside the patterned array were removed by gentle sonication, resulting in arrays of parallel NWs at desired locations (Fig. 103). To produce crossed NW arrays, sequential layers of aligned NWs were transferred in an orthogonal orientation and were patterned in the same fashion as described above (Fig. 103). Fig. 103(C) shows an image of a 10μm×10 μm square array with a 25μmarray pitch, and demonstrates that such a method provides ready and scalable access to ordered arrays over large areas. The nanowire array exhibits order on multiple length scales: 40nm diameter NWs, 0.5μm NW spacing, 10μm array size, 25μm array pitch repeated over centimetres—that is representative of the substantial control enabled by the LB approach. Array geometries and tiling patterns more complex than square structures are also believed to be

achievable.

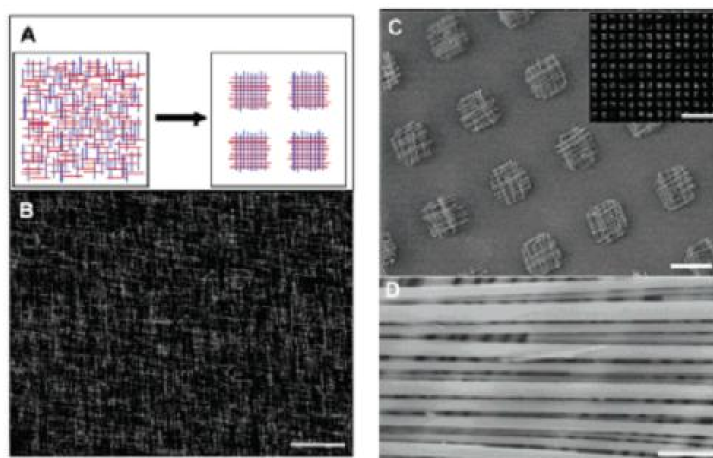


Figure 7 (A) Hierarchical patterning of crossed NW arrays by photo-lithography, where NWs are removed from regions outside of the defined array pattern. (B) Dark-field optical micrograph of crossed NWs deposited uniformly on a 1 cm × 1 cm substrate. Scale bar: 50 μm. (C) SEM image of patterned crossed NW arrays. Scale bar: 10 μm. (Inset) Large area dark-field optical micrograph of the patterned crossed NW arrays. Scale bar: 100 μm. (D) SEM image of an ultra-high density crossed NW array. Scale bar: 200 nm.

【Gambino J P and Colgan E G 1998 Mater. Chem. Phys. 52 99】

6.7 Conclusion

The area of semiconductor NWs has been constantly gaining interest and momentum among science and engineering communities since the late 1990s. In this review, we attempted to summarize progresses made in this field during the last several years, ranging from nanowire growth with precise control at the atomic level to device characterization that probes novel properties in 1D systems and novel device structures, and to integration and assembly methods of large numbers of NWs for practical applications. The key ingredients in the semiconductor nanowire system include the single-crystalline nature of the material, strong quantum confinement effects due to the small diameter and the ability to carry out tailored growth with desired shape, size and material composition (including radial and axial nanowire heterostructures). The separation of high-temperature growth and low-temperature device fabrication processes also implies that nanowire devices are well suited to applications on non-crystalline substrates such as flexible electronics. Because of their high carrier mobility and large surface

area, semiconductor NWs have also been studied in a variety of applications besides high-performance electronics, including dye-sensitized solar cells, label-free, ultrasensitive bio-and chemical sensors. By exploiting the optical cavity and/or waveguide properties of the semiconductor material, nanowire-based on-chip photonic devices and circuits have been demonstrated as well, including light-emitting diodes, lasers, active waveguides and integrated electro-optic modulators. Such topics are beyond the scope of this reviewand interested readers are referred to the corresponding references listed above.

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